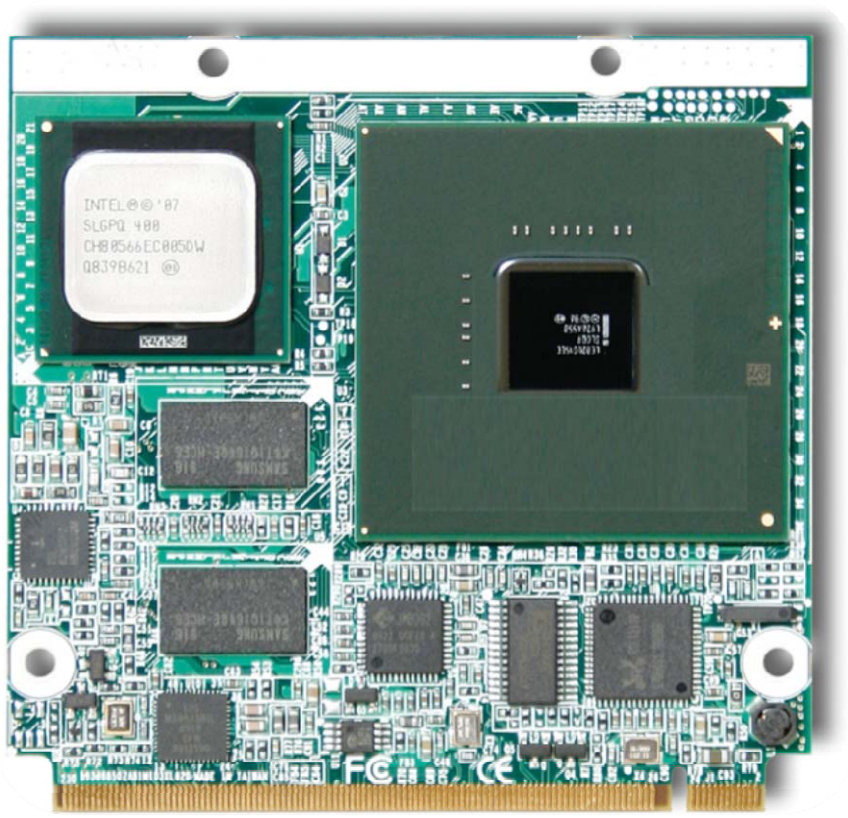
PQ7-M103XL Series

User's Manual



Version 1.0

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Appendix A

Appendix B

How to Use This Manual

The manual describes how to configure your PQ7-M103XL series to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of this Q7 Module.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this model of single board computer.

Chapter 2 : Hardware Configuration. Describes the definition and location for Jumpers that you can easily configure your system.

Chapter 3 : System Installation. Describes the CPU, main memory SKU to get a clear information.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

The content of this manual and EC declaration document is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site : http://www.portwell.com.tw

Chapter 1
System Overview

1.1 Introduction

QSEVEN, a new industrial computer platform in "Module board" and "Carrier board" architecture, equipped processor or its socket, chipset, memory or memory socket and single Ethernet controller on it. The On-The-Shelf Module board allows users to create their own Carrier board easily and quickly since most critical parts are ready on Module board. QSEVEN Module board offers expansion interfaces such as PCI Express, SATA, LPC, LVDS, USB, SDVO and Audio etc. that could support variety functions depending on Carrier board design.

The Carrier board was customized design to fit in different mechanical requirements. In the meanwhile, its variety functions were also customized to meet the application. Compares to the platform that designed from nothing, QSEVEN architecture platform only needs to develop Carrier board. Users could keep their know-how which related to their core competence in the Carrier board.

PQ7-M103XL series equipped Intel eMenlow XL chipset with Atom Z510PT/Z520PT processor on-board), 512 MB DDR2 memories (up to 1GB) on-board, one Gigabit Ethernet controller on it to provide expansion interfaces – PCI Express x1.

1.2 Check List

The PQ7-M103XL series package should cover the following basic items

One PQ7-M103XL series module board

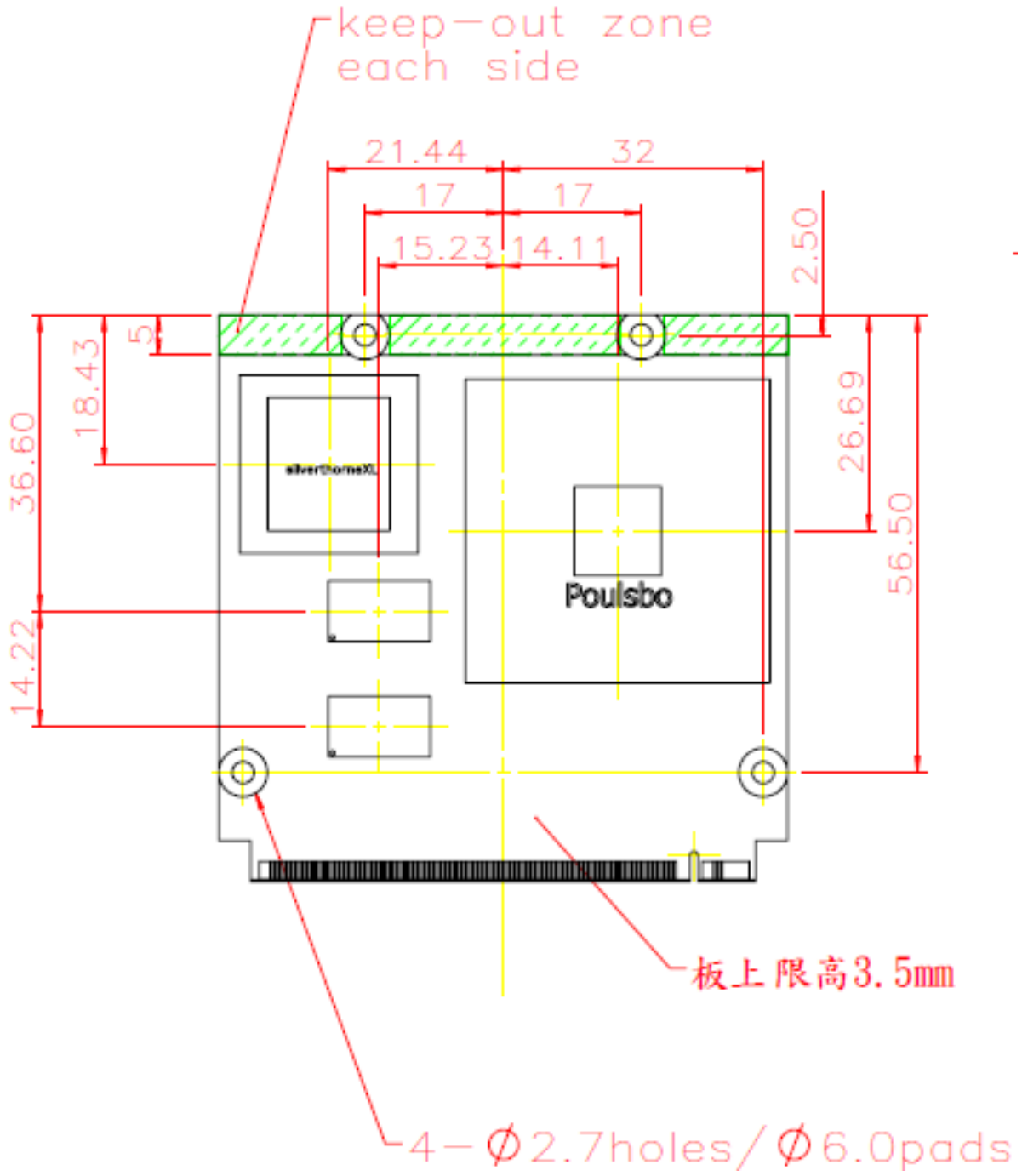
If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

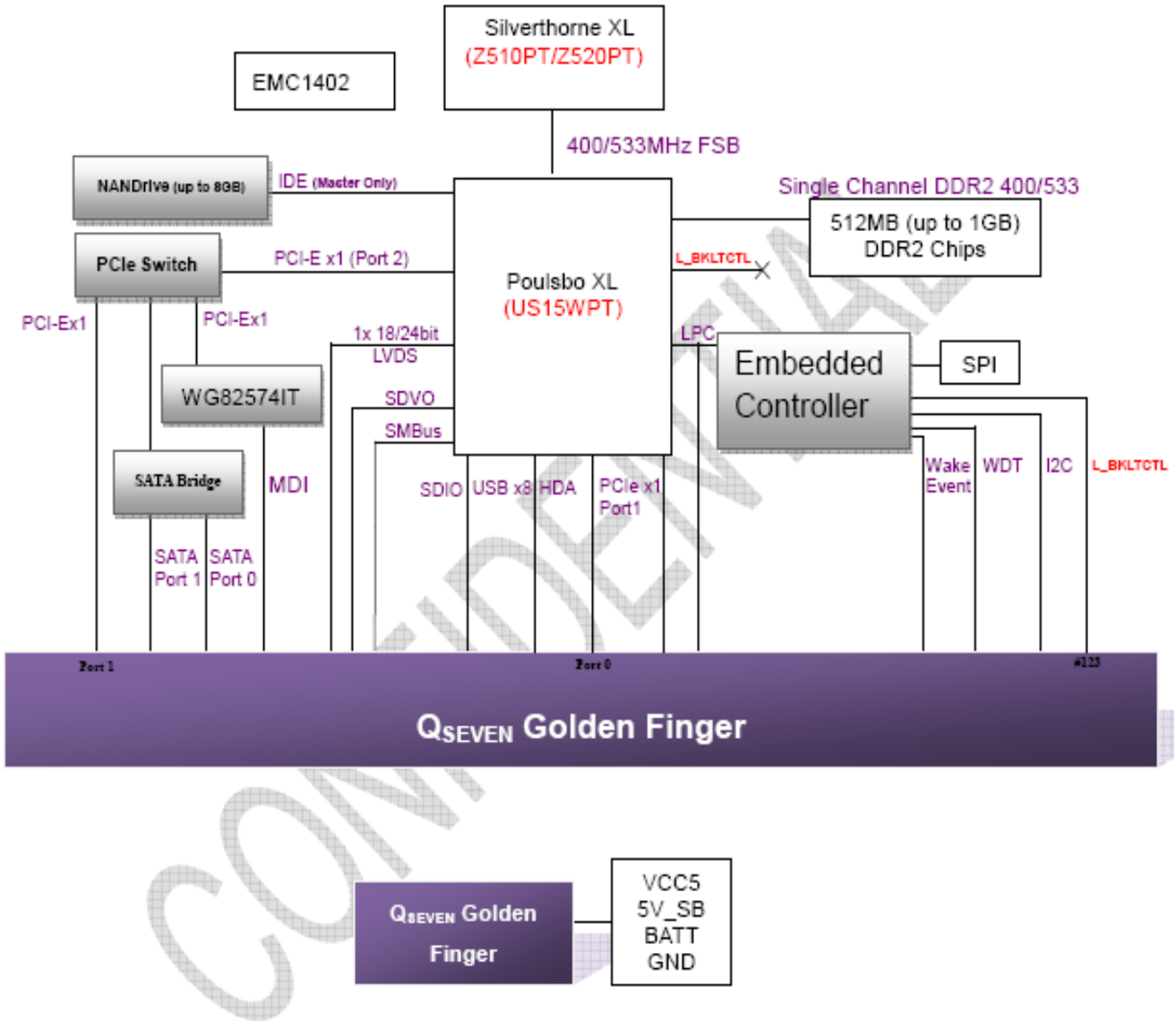
- **Main processor**
  - Intel® Atom Processor
  - FSB: Z510PT 400MHz; Z520PT 533MHz
- **Main Memory**
  - Onboard DDR2 400/533 up to 1GB
- **L2 Cache Memory**
  - 512K L2 Cache, Build-in processor
- **Chipset**
  - Intel eMenlow (US15WPT) chipset
- **Expansion Interfaces**
  - PCI Express
    - Two PCI Express x1 links (Up to three links if no SATA demand)
  - LVDS
    - Supports maximum 112MHz single channel LVDS interface
    - Single channel LVDS interface support: 24 bpp
    - Maximum Panel resolution supported up to 1366 x 768
  - SDVO (Serial Digital Video Output)
    - A maximum pixel clock of 160 MHz is supported on the SDVO interface.
  - Ethernet
    - Intel WG82574IT Gigabit Ethernet controller is equipped
  - USB Interface
    - Support eight USB 2.0 ports
  - IDE Interface
    - Support 4GB NANDrive storage onboard, up to 8GB capacity.

- **Outline Dimension (L X W):**
  - 70mm x 70mm
- **Operating Temperature:**
  - 40°C ~ 85°C
- **Storage Temperature:**
  - 40°C ~ 85°C
- **Relative Humidity:**
  - 5% ~ 90%, non-condensing

1.4 Mechanical Drawing



1.5 System Architecture



PQ7-M103XL Series System Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connector. All of the configuration jumpers on Portwell EVB Carrier PQ7-M103XL are in the proper position. The default settings shipped from factory are marked (★).

2.1 Jumper Setting

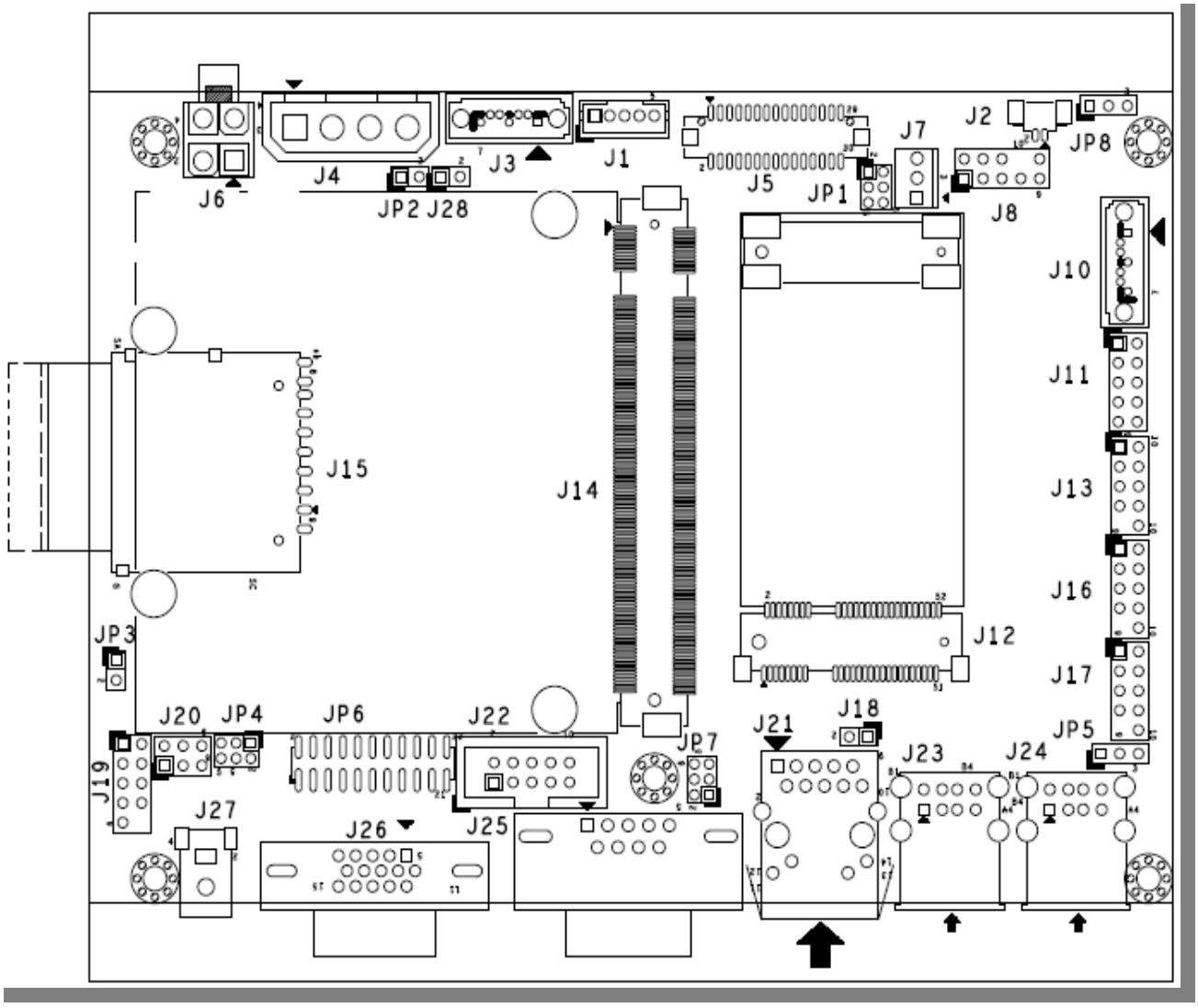


Figure 2-1 PQ7-M103XL Jumper & Connector Location

JP1 : LVDS Power Level

JP1	Process Selection
1-3	3.3V ★
3-4	12V
3-5	5V

JP2 : CPU Board BIOS Disable

JP2	Function
1-2	BIOS Disable

JP3 : Auto Power Button selection

JP3	Function
1-2	Auto power button mode

JP4 : RTC CMOS Clear Jumper Setting

JP4	Function
1-3、2-4	For com port ★
3-5、4-6	For IrDA

JP5 : USB Host/Client Select

JP5	Function
1-2	Host ★
2-3	Client

JP6 : COM2 RS232/485/422 Selection

JP6	Function
RS232	5-6,9-11,10-12,15-17,16-18 ★
RS485	1-2,7-9,8-10,19-20
RS422	3-4,7-9,8-10,13-15,14-16,21-22

JP7 : LVDS Back-light Power Level

JP7	Process Selection
1-3,2-4	5V, Active High ★
1-3,4-6	12V, Active High
3-5,2-4	5V, Active Low
3-5,4-6	12V, Active Low

JP8 : CMOS Reset

JP8	Function
1-2	Normal Operation ★
2-3	Clear CMOS Contents

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors.

Connector Function List

Connector	Function	Remark
J1	LVDS Panel Back-light Power Connector	
J2	RTC Battery Connector	
J3/10	SATA Interface Connector	
J4	Power Header	
J5	LVDS Connector	
J6	4P Power Connector for 12V	
J7	3P FAN Power Connector (System)	
J8	Audio Header	
J11	8-Bit GPIO Header	
J12	Mini-PCI E Connector	
J13	LPC Debug Port	
J14	MXM Connector	
J15	SD Card Slot	
J16	Dual Port USB Header (Only USB2.0 Device)	
J17	Client USB Header	
J19	Front Panel Control Header	
J20	IrDA Connector	
J21	RJ45 Lan Port	
J22	COM2 Serial Port BOX Header	
J23/J24	Dual Port USB	
J25	COM 1 Serial Port Connector	
J26	D-Sub15 VGA Connector	
J27	DC Jack 12V	
J28	Reserve Header	

Pin Assignments of Connectors

J1 : LVDS Panel Back-light Power Connector

PIN No.	Signal Description
1	Backlight Power
2	Ground
3	+12V
4	L_BKLTCTL
5	+5V

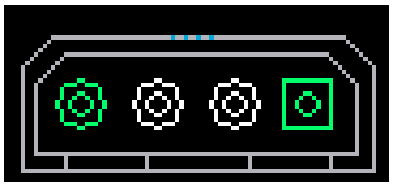
J2 : RTC Battery Connector

PIN No.	Signal Description
1	Positive
2	Negative

J3/10 : SATA Interface Connector

PIN No.	Signal Description	
1	GND	GND
2	SATA_TXP0	SATA_TXP1
3	SATA_TXN0	SATA_TXN1
4	GND	GND
5	SATA_RXN0	SATA_RXN1
6	SATA_RXP0	SATA_RXP1
7	GND	GND

J4 : Power Header

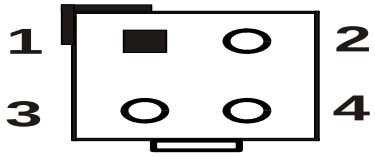


PIN No.	Signal Description
1	V12
2	GND
3	GND
4	VCC

J5 : LVDS Panel Connector

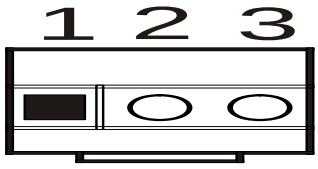
PIN No.	Signal Description	PIN No.	Signal Description
1	VDD_LVDS	2	VDD_LVDS
3	DF_LA_DATA+0	4	DF_LA_DATA-0
5	DF_LA_DATA+1	6	DF_LA_DATA-1
7	DF_LA_DATA+2	8	DF_LA_DATA-2
9	DF_LA_DATA+3	10	DF_LA_DATA-3
11	DF_LA_CLK+	12	DF_LA_CLK-
13	L_CTLA_CLK	14	L_CTLB_DATA
15	GND	16	GND
17	DF_LB_DATA+0	18	DF_LB_DATA-0
19	DF_LB_DATA+1	20	DF_LB_DATA-1
21	DF_LB_DATA+2	22	DF_LB_DATA-2
23	DF_LB_DATA+3	24	DF_LB_DATA-3
25	DF_LB_CLK+	26	DF_LB_CLK-
27	N/A	28	N/A
29	GND	30	GND

J6 : 4P Power Connector for 12V



PIN No.	Signal Description
1	Ground
2	Ground
3	+12V
4	+12V

J7 : 3P FAN Power Connector



PIN No.	Signal Description
1	Ground
2	+12V
3	Fan Speed Detecting signal

J8 : Audio Header

PIN No.	Signal Description
1	CN_MIC-R
2	AGND
3	CN_MIC-L
4	AGND
5	CN_LINOUT-R
6	NC
7	VCC
8	
9	CN_LINOUT-L
10	NC

J11 : 8-Bit GPIO Header

PIN No.	Signal Description	PIN No.	Signal Description
1	SIO_GPIO0	2	SIO_GPIO4
3	SIO_GPIO1	4	SIO_GPIO5
5	SIO_GPIO2	6	SIO_GPIO6
7	SIO_GPIO3	8	SIO_GPIO7
9	Ground	10	VCC

J12 : Mini-PCIE Slot

PIN No.	Signal Description	PIN No.	Signal Description
1	PCIE_WAKE#	2	VCC3
3	N/C	4	GND
5	N/C	6	VCC1_5
7	CLKREQ#	8	N/C
9	GND	10	N/C
11	DF_CLK_PCIE#	12	N/C
13	DF_CLK_PCIE	14	N/C
15	GND	16	N/C
17	N/C	18	GND
19	N/C	20	N/C
21	GND	22	RST#
23	DF_PCIE_RXN1	24	3.3VAUX
25	DF_PCIE_RXP1	26	GND
27	GND	28	VCC1_5
29	GND	30	SMB_CLK
31	DF_PCIE_TXN1	32	SMB_DAT
33	DF_PCIE_TXP1	34	GND
35	GND	36	DF_USB_PN0

37	N/C	38	DF_USB_PP0
39	N/C	40	GND
41	N/C	42	N/C
43	N/C	44	N/C
45	N/C	46	N/C
47	N/C	48	VCC1_5
49	N/C	50	GND
51	N/C	52	VCC3

J13 : LPC Debug Port

PIN No.	Signal Description	PIN No.	Signal Description
1	LPC_AD0	2	VCC3
3	LPC_AD1	4	RST#
5	LPC_AD2	6	LPC_FRAME#
7	LPC_AD3	8	CLK_LPC_FWH
9		10	GND

J14 : MXM Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GND	2	GND
3	DF_LAN1_MDIN3	4	DF_LAN1_MDIN2
5	DF_LAN1_MDIP3	6	DF_LAN1_MDIP2
7	LAN1_LINK100-	8	LAN1_LINK1000-
9	DF_LAN1_MDIN1	10	DF_LAN1_MDIN0
11	DF_LAN1_MDIP1	12	DF_LAN1_MDIP0
13	LAN1_LINK#	14	LAN1_ACT-
15	VCTREF_GBE0_CT	16	SLP_S5#
17	LPC_PME#	18	SLP_S3#
19	VSB3	20	PWRBTN#_PM
21	**SLP_BTN# (not implement)**	22	**LID_BTN# (not implement)**
23	GND	24	GND
25	GND	26	PWROK_Q7
27	**BATLOW# (not implement)**	28	RST_SYS#
29	DF_SATA0_TX+	30	DF_SATA1_TX+
31	DF_SATA0_TX-	32	DF_SATA1_TX-
33	SATA_ACT#	34	GND
35	DF_SATA0_RX+	36	DF_SATA1_RX+
37	DF_SATA0_RX-	38	DF_SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE#	42	SLOT2_CLK
43	SLOT2_CD#	44	SD2_LED
45	SLOT2_CMD	46	SLOT2_WP
47	SD2PWR#	48	SLOT2_DATA1
49	SLOT2_DATA0	50	SLOT2_DATA3
51	SLOT2_DATA2	52	**SLOT2_DATA5**
53	**SLOT2_DATA4**	54	**SLOT2_DATA7**
55	**SLOT2_DATA6**	56	**RSVD**
57	GND	58	GND
59	HAD_SYNC	60	SMB_CLK
61	HAD_RST#	62	SMB_DATA
63	HAD_BITCLK	64	**SMB_ALERT#**
65	HAD_SDATAIN0	66	I2C_CLK
67	HAD_SDATAOUT	68	I2C_DAT
69	PM_THRM#	70	**WDTRIG#**
71	**THERMTRIP#**	72	**WDOUT (not implement)**
73	**GND**	74	GND
75	DF_USB_PN7	76	DF_USB_PN6
77	DF_USB_PP7	78	DF_USB_PP6
79	USB_6_7_OC#	80	USB_4_5_OC#
81	DF_USB_PN5	82	DF_USB_PN4

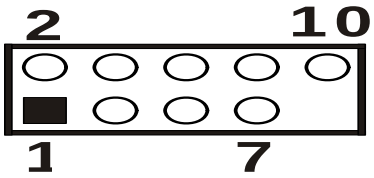
83	DF_USB_PP5	84	DF_USB_PP4
85	USB_2_3_OC	86	USB_0_1_OC#
87	DF_USB_PN3	88	DF_USB_PN2
89	DF_USB_PP3	90	DF_USB_PP2
91	**USB_HOST_PRES#**	92	**USB_HC_SEL**
93	DF_USB_PN1	94	DF_USB_PN0
95	DF_USB_PP1	96	DF_USB_PP0
97	GND	98	GND
99	LA_DATAP0	100	LB_DATAP0 **(not implement)**
101	LA_DATAN0	102	LB_DATAN0 **(not implement)**
103	LA_DATAP1	104	LB_DATAP1 **(not implement)**
105	LA_DATAN1	106	LB_DATAN1 **(not implement)**
107	LA_DATAP2	108	LB_DATAP2 **(not implement)**
109	LA_DATAN2	110	LB_DATAN2 **(not implement)**
111	L_VDDEN	112	L_BKLTEN
113	LA_DATAP3	114	LB_DATAP3 **(not implement)**
115	LA_DATAN3	116	LB_DATAN3 **(not implement)**
117	GND	118	GND
119	DF_LA_CLKP	120	DF_LB_CLKP **(not implement)**
121	DF_LA_CLKN	122	DF_LB_CLKN **(not implement)**
123	L_BKLTCTL	124	**RSVD**
125	**LVDS_DID_DAT**	126	LVDS_BLC_DAT
127	**LVDS_DID_ CLK**	128	LVDS_BLC_CLK
129	**RSVD**	130	**RSVD**
131	SDVO_CLK+	132	**SDVO_INT+**
133	SDVO_CLK-	134	**SDVO_INT-**
135	GND	136	GND
137	SDVO_GREEN+	138	**SDVO_FLDSTALL+**
139	SDVO_GREEN-	140	**SDVO_FLDSTALL-**
141	GND	142	GND
143	SDVO_BLUE+	144	SDVO_TVCLKIN+
145	SDVO_BLUE-	146	SDVO_TVCLKIN-
147	GND	148	**GND**
149	SDVO_RED+	150	SDVO_CTRLDATA
151	SDVO_RED-	152	SDVO_CTRLCLK
153	N/C	154	N/C
155	DF_CLK_PCIE+	156	PCIE_WAKE#
157	DF_CLK_PCIE-	158	RST#
159	GND	160	GND
161	**PCIE_TX3+ (not implement)**	162	**PCIE_RX3+(not implement)**
163	**PCIE_TX3- (not implement)**	164	**PCIE_RX3- (not implement)**
165	GND	166	GND
167	**PCIE_TX2+ (not implement)**	168	**PCIE_RX2+(not implement)**
169	**PCIE_TX2- (not implement)**	170	**PCIE_RX2- (not implement)**
171	EXCD0_PERST#	172	EXCD1_PERST#

173	**PCIE_TX1+**	174	**PCIE_RX1+**
175	**PCIE_TX1-**	176	**PCIE_RX1-**
177	**EXCD0_CPPE# (not implement)**	178	**EXCD1_CPPE# (not implement)**
179	**PCIE_TX0+**	180	**PCIE_RX0+**
181	**PCIE_TX0-**	182	**PCIE_RX0-**
183	GND	184	GND
185	LPC_AD0	186	LPC_AD1
187	LPC_AD2	188	LPC_AD3
189	CLK_LPC_FWH	190	LPC_FRAME#
191	LPC_SERIRQ	192	**LPC_LDRQ#(not implement)**
193	V3.3A_RTC	194	SPKR
195	**FAN_TACHOIN (not implement)**	196	**FAN_PWMOUT (no implement**
197	GND	198	GND
199	**RSVD**	200	**RSVD**
201	**RSVD (use for A20M#)**	202	**RSVD**
203	**RSVD**	204	MFG_N/C
205	VSB5	206	VSB5
207	MFG_N/C	208	MFG_N/C
209	MFG_N/C	210	MFG_N/C
211	VCC	212	VCC
213	VCC	214	VCC
215	VCC	216	VCC
217	VCC	218	VCC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

J15 : SD Card Slo

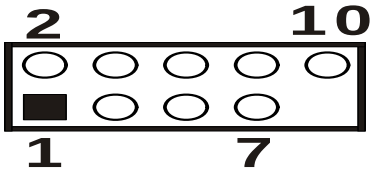
PIN No.	Signal Description
1	DAT3
2	CMD_RSP
3	GND
4	VCC
5	CLK
6	GND
7	DAT0
8	DAT1
9	DAT2
Sa	WP#
Sb	CD#
Sc	CD#_COM

J16 : Dual Port USB Header(Only USB2.0 Device)



PIN No.	Signal Description	PIN No.	Signal Description
1	+5V	2	+5V
3	USBD6N	4	USBD7N
5	USBD6P	6	USBD7P
7	Ground	8	Ground
		10	NC

J17 : Client USB Header



PIN No.	Signal Description	PIN No.	Signal Description
1	+5V	2	NC
3	USBD1N	4	NC
5	USBD1P	6	NC
7	Ground	8	NC
		10	NC

J19 : Front panel Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	HD_LED_P	2	FP PWR/SL_P
3	HD_LED_N	4	FP PWR/SL_N
5	RST_SW_N	6	PWR_SW_P
7	RST_SW_P	8	PWR_SW_N
9	RSVD_DNU	10	

J20 : IrDA Connector

PIN No.	Signal Description
1	IRRX
2	Ground
3	Ground
4	NC
5	IRTX
6	VCC

J21 : RJ45 LAN Port

PIN No.	Signal Description
1	L1_MDIP0
2	L1_MDIN0
3	L1_MDIP1
4	L1_MDIN1
5	VCTREF_GBE0_CT
6	GND
7	L1_MDIP2
8	L1_MDIN2
9	L1_MDIP3
10	L1_MDIN3
11	LAN1_ACT-
12	LAN1_LINK#
13	LAN1_LINK1000-
14	LAN1_LINK100-

J22 : COM2 Serial Port BOX Header

PIN No.	Signal Description	PIN No.	Signal Description
1	DCD#2	2	DSR#2
3	RXD#2	4	RTS#2
5	TXD#2	6	CTS#2
7	DTR#2	8	RI#2
9	GND	10	

J23 : Dual Port USB

PIN No.	Signal Description	PIN No.	Signal Description
A1	+5V	B1	+5V
A2	USBD3N	B2	USBD2N
A3	USBD3P	B3	USBD2P
A4	Ground	B4	Ground

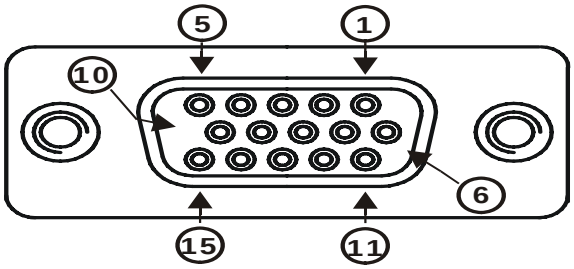
J24 : Dual Port USB

PIN No.	Signal Description	PIN No.	Signal Description
A1	+5V	B1	+5V
A2	USBD5N	B2	USBD4N
A3	USBD5P	B3	USBD4P
A4	Ground	B4	Ground

J25 : COM 1 Serial Port Connector

PIN No.	Signal Description		
	RS-232	**RS-422**	**RS-485**
1	DCD (Data Carrier Detect)	TX-	DATA-
2	RXD (Receive Data)	TX+	DATA+
3	TXD (Transmit Data)	RX+	N/C
4	DTR (Data Terminal Ready)	RX-	N/C
5	GND (Ground)	GND	GND
6	DSR (Data Set Ready)	N/C	N/C
7	RTS (Request to Send)	N/C	N/C
8	CTS (Clear to Send)	N/C	N/C
9	RI/5V/12V	N/C	N/C

J26 : D-SUB15 VGA Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	RED	2	GREEN
3	BLUE	4	ID0
5	Ground	6	Ground
7	Ground	8	Ground
9	NC	10	Ground
11	ID1	12	DDCDATA
13	HSYNC	14	VSYNC
15	DDCCLK		

J27 : DC Jack 12V

PIN No.	Signal Description
2	V12CON_IN
3	GND
4	GND

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel ATOM processor Z510PT/Z520PT CPU

Configuring System Bus

PQ7-M103XL will automatically detect the CPU FSB 400/533MHz CMOS used. CPU speed of Intel ATOM Processor for Mobile can be detected automatically.

3.2 Intel System Controller Hub US15WPT

The Intel® System Controller Hub US15WPT is a low-power chipset in one small 22x22mm package; it combines the Intel® Graphics Media Accelerator 500, memorycontroller, and I/O controller in a single-chip solution while featuring advanced 3D graphics and extensive I/O capabilities such as USB2.0, SDIO and PCI Express. It supports Intel® High Definition Audio and hardware video decode acceleration, a 400/533 MHz CMOS front-side bus, dual independent display.

3.3 Main Memory

PQ7-M103XL provides 1 GBytes of on-board DDR2-SDRAM as main memory. Memory clock and related settings can be detected by BIOS via SPD interface.

Memory frequency / CPU FSB synchronization
PQ7-M103XL supports different memory frequencies depending on the CPU front side bus and the type of DDR2-SDRAM.

CPU FSB	Memory Frequency
533MHz	533MHz
400MHz	400MHz

3.4 Installing the Single Board Computer

To install your PQ7-M103XL into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure CPU and memory module on right position
Step 3 : Place PQ7-M103XL into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING
Please ensure that SBC is properly inserted and fixed by mechanism.

Note:
Please refer to section 3.4.1 to 3.4.4 to install INF/VGA/LAN/Audio drivers

3.4.1 Chipset Component Driver

The chipset on PQ7-M103XL is a new chipset that a few old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows XP/VISTA, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in PQ7-M103XL CD-title.

3.4.2 Intel Integrated Graphics GMCH Chip

Using Intel® SCH US15WPT with Media Accelerator High performance graphic integrated chipset is aimed to gain an outstanding graphic performance. Shared 1MB to 8MB system DDR2-SDRAM Memory with Total Graphics Memory. This combination makes PQ7-M103XL an excellent piece of multimedia hardware.

Drivers Support
Please find Springdale GMCH driver in the PQ7-M103XL CD-title. Drivers support Windows XP / VISTA.

3.4.3 Intel Gigabit Ethernet Controller

Drivers Support
Please find WG82574IT LAN driver in /Ethernet directory of PQ7-M103XL CD-title. The drivers support Windows XP / VISTA.

LED Indicator (for LAN status)
PQ7-M103XL provides two LED indicators to report WG82574IT Gigabit Ethernet interface status. Please refer to the table below as a quick reference guide.

<table>
<tr><th rowspan="2">Intel 82574IT</th><th rowspan="2">Color</th><th rowspan="2">Name of LED</th><th colspan="3">Operation of Ethernet Port</th></tr>
<tr><th colspan="2">Linked</th><th>Active</th></tr>
<tr><td>Status LED</td><td>Green</td><td>Linked & Active LED</td><td colspan="2">On</td><td>Blinking</td></tr>
<tr><td rowspan="2">Speed LED</td><td>Orange</td><td rowspan="2">Speed LED</td><td>Giga Mbps</td><td>100 Mbps</td><td>10 Mbps</td></tr>
<tr><td>Green</td><td>Orange</td><td>Green</td><td>Off</td></tr>
</table>

3.4.4 Audio Controller

Please find Realtek ALC262 Audio driver form PQ7-M103XL CD-title. The drivers support Windows XP / VISTA.

3.5 Installing the Single Board Computer

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

JP8 : CMOS Reset

JP8	Function
1-2	Normal Operation ★
2-3	Clear CMOS Contents

To correctly operate CMOS Clear function, users must turn off the system, move JP8 jumper to short pin 2 and 3. Move the JP8 back to 1-2 position (Normal Operation) and start the system. System will then produce a "CMOS Check Sum Error" message and hold up. Users may then follow the displayed message to load BIOS default setting.

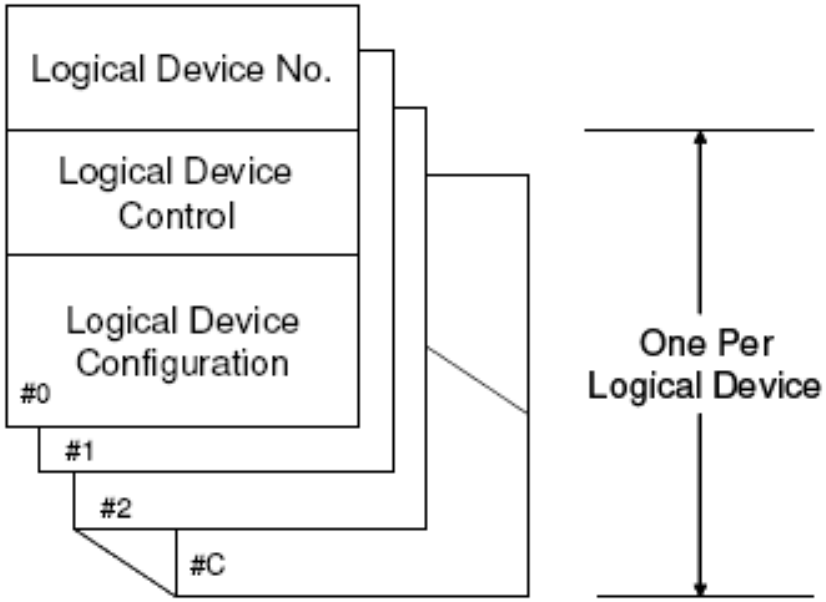
3.6 WDT Function

The algorithm of the WDT function can be simply described as a timer counting process with an output event. The Time-Out period (T_{wd}) can be set by software commands or hardware jumpers that depend on the board circuit design and may be different among the boards. This timer can be used to monitor a software hang.

PQ7-M103XL allows users to control WDT by issuing dynamic software commands. The WDT starts counting when it is activated. It will cause a system reset once it expires. Before WDT expires, a refreshing command with a T_{wd} can be issued to re-count WDT and continue the status monitoring. If the system encounters a software or application hang, WDT will generate a system reset after its timeout.

The related Control Registers of WDT are included in the following programming guide that is written in C language. User can write a non-zero value (defined as T_{wd}) into the Time-out Value Register (CR_T_{wd}) to enable WDT. Users can write 0x00 and then T_{wd} to CR_T_{wd} to refresh WDT. To refresh WDT, the time tolerance of refreshing interval must be considered. The smaller of T_{wd}, the more deviation of WDT and you need to include more tolerance. "Let T_{wd} be longer than 2 seconds" is the recommendation due to the limitation of Winbond W83627DHG WDT. You can call Portwell support center for reference. The value read back from CR_T_{wd} indicates the counting down value instead of the original T_{wd}. System will be reset after the Time-out Value to be counted down to zero. Users can directly fill a zero value into CR_T_{wd} to disable WDT immediately. To ensure a successful access to the desired Control Register, the following programming guide should be followed.

Programming guide:
CR: Configuration Register.
LD: Logical Device of SIO. There are 12 LDs in W83627DHG SIO.
CR00~2F: Global Control Registers. (All LDs share these CRs)
CR07: LD selection.
CR30~FF: Each LD has its own CR30~FF.



There are two I/O ports as I/O access window for configuring WDT,
1) IO port 0x2E is H/W strapped and named as EFIR (Extended Function Index Register, for identifying CR index number)
2) IO port 0x2F is H/W strapped and named as EFDR (Extended Function Data Register, for accessing desired CR)

<< How to access W83627DHG Configuration Register >>
First, it needs to enter extended function mode.
Enter extended function mode for accessing W83627DHG configuration registers:
outportb (EFIR, 0x87);
outportb (EFIR, 0x87); // double IO write

Read Configuration Register CR_rx, and keep this byte to unsigned char al_char
outportb(EFIR, CR_rx) ;
al_char = inportb(EFDR) ;
Write Configuration Register CR_wx with byte al_char1 ;
outportb (EFIR, CR_wx) ;
outportb (EFDR, al_char1);
Exit extended mode after completion of configuration register access.
outportb(EFIR, 0xaa);

<< How to access W83627DHG WDT Configuration Register >>
Must enter extended function mode first, then follow the following steps for accessing WDT registers.

Step (1): CR2D_bit0P0
Initialize the multiplex pin (pin77) to WDTO function
outportb (EFIR , 0x2D) ; // al_char1 : unsigned char
al_char1 = inportb (EFDR) & 0xFE; // CR2D_bit0P0
outportb (EFIR , 0x2D) ; // init pin 77 to WDT
outportb (EFDR , al_char1) ;

Step (2) : CR07_P08
Ponit to LD8.
outportb (EFIR , 0x07) ;
outportb (EFDR , 0x08) ;

Step (3) : LD8_CR30_bit0P1
Activate LD8
outportb (EFIR , 0x30) ;
al_char1 = inportb (EFDR) | 0x01 ; // CR30_bit0P1
outportb (EFIR , 0x30) ; // Activate LD8
outportb (EFDR , al_char1) ;

Step (4) : LD8_CRF7_bit[7,6]P[0,0]
Not allow K/B and Mouse's interrupts to reload WDT timer.
outportb (EFIR , 0xF7) ;
al_char1 = inportb (EFDR) & 0x3F ; // CRF7_bit[7,6]P[0,0]
outportb (EFIR , 0xF7) ;
outportb (EFDR , al_char1) ;

Step (5) : Refresh WDT before it expires.
Once WDT expires, system will be reset.
LD8_CRF5_bit3 :
0 : Second Mode
1 : Minute Mode
LD8_CRF6: T_{wd} , "Writing 00" means "disable WDT"
1~255 time unit (time unit: second, minute)

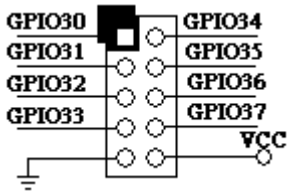
Notes:
"CR2D_bit0P0"means" Write 0 to bit0 of Configuration Register 0x2D".

3.7 GPIO

The PQ7-M103XL provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

The GPIO ports are located on J12 shown as follows.
Notes : **Do not short-circuit Pin 9 and 10 of J11 !**

J11: GPIO Connector (2*5 Pin Header)



J11: General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	Ground	10	+5V

Programming Guide:
Must enter extended function mode (Double I/O write 0x87 to EFIR) first, then follow the following steps for accessing GPIO pins. When completion of GPIO access, Exit extended mode (I/O write 0xaa to EFIR).

Initialize W83627DHG multiplex pins as GPIO30~37 pins
CR2C_bit[7:5]P[0,0,0]

```
outportb ( EFIR , 0x2C ) ;          // al_char1 : unsigned char
al_char1 = inportb ( EFDR ) | 0x02 ;  // CR2C_bit[7:5]P[0,0,0]
outportb ( EFIR , 0x2C ) ;          // init GP30~37 function
outportb ( EFDR , al_char1 ) ;
```

Point to LD9 and activate its function

```
CR07_P09       ; Point to LD9
outportb ( EFIR , 0x09 ) ;
outportb ( EFDR , 0x09 ) ;
LD9_CR30_bit1P1  ; Activate LD9
outportb ( EFIR , 0x30 ) ;
al_char1 = inportb ( EFDR ) | 0x02 ;  // CR30_bit1P1
outportb ( EFIR , 0x30 ) ;          // Activate LD9
outportb ( EFDR , al_char1 ) ;
```

(1) LD9_CRF2_PFF ; Inverse input/output signals

```
outportb ( EFIR , 0xF2 ) ;
outportb ( EFDR , 0xFF ) ;
```

(2) LD9_CRF0_PF0 ; Set GP30~33 as input pins and GP34~37 as output pins

```
outportb ( EFIR , 0xF0 ) ;
outportb ( EFDR , 0xF0 ) ;
```

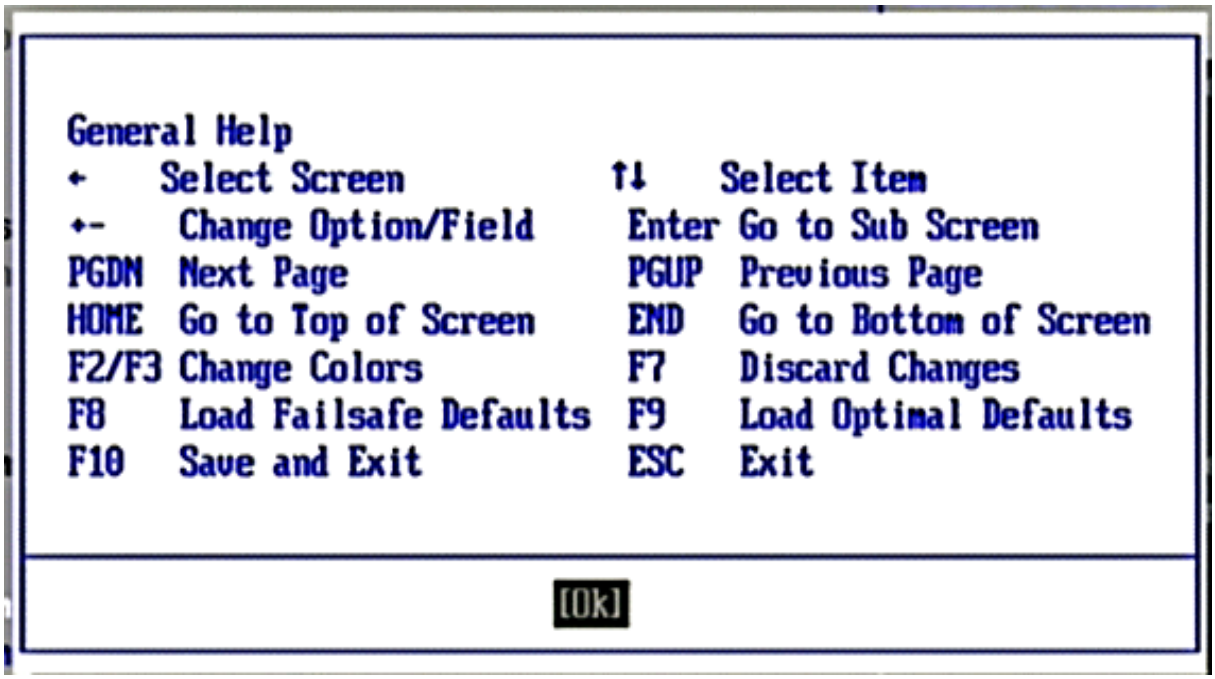
(3) LD9_CRF1 ; Data Register for reading/writing data to GPIO pins
; E.g. if put four jumper caps on J12 pin1-2,3-4,5-6,and 7-8
; (Warning : J22 pin9-10 is not allowed to be short circuit.)
; and then Write [1,0,1,0] to bit[3:0] , you can get [1,0,1,0]
; from bit[7:4].

Chapter 4
BIOS Setup Information

PQ7-M103XL is equipped with the AMI BIOS stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, PQ7-M103XL communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

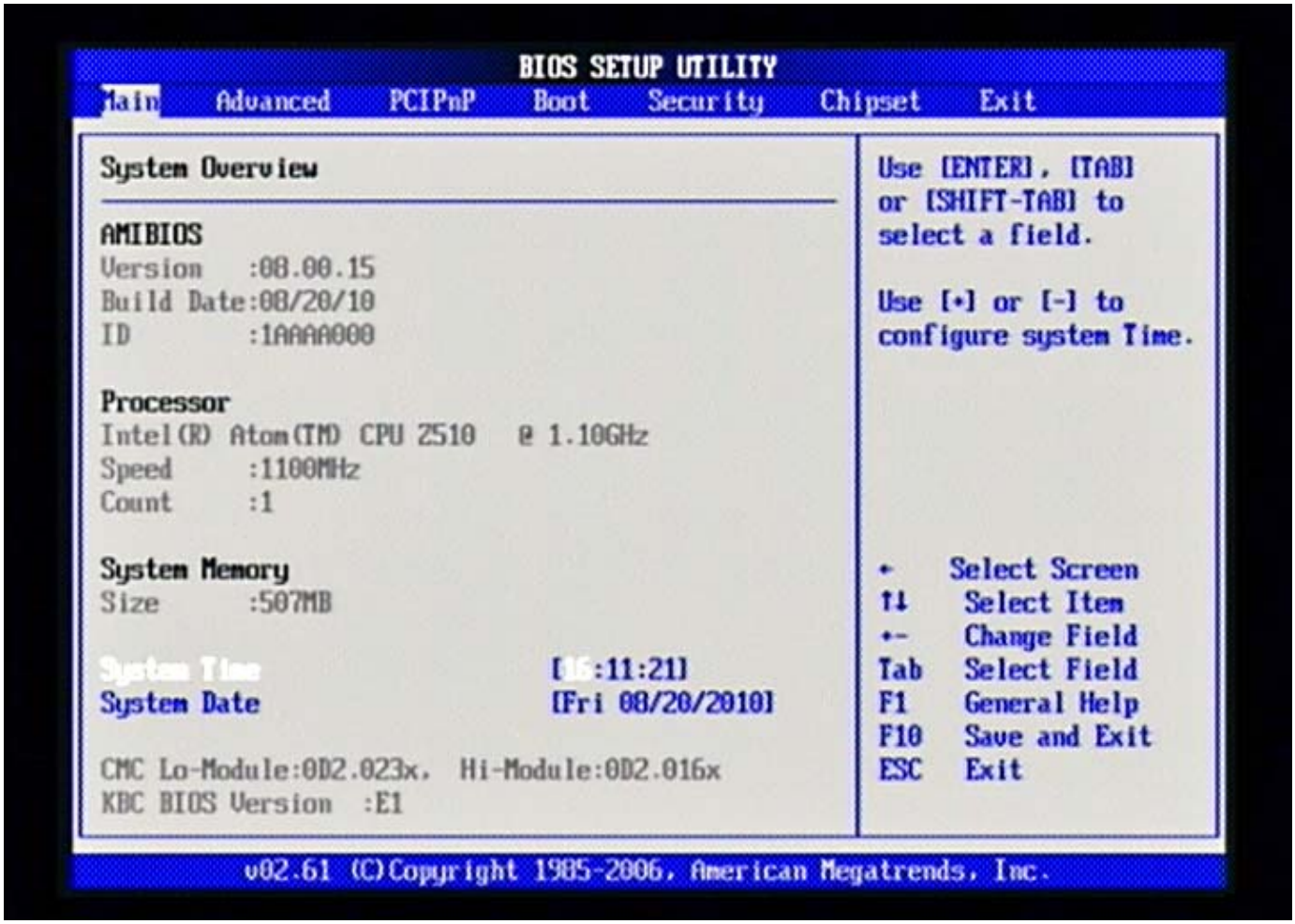
4.1 Entering Setup -- Launch System Setup

Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key to enter Setup.
Press <Del> to enter SETUP
If the message disappears before you respond and you still wish to enter Setup, restart the system by turning it OFF and On or pressing the RESET button. You may also restart the system by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys.
Press <F1> to Run SETUP or Resume
The BIOS setup program provides a General Help screen. You can call up this screen from any menu by simply pressing <F1>. The Help screen lists the appropriate keys to use and the possible selections for the highlighted item. Press <Esc> to exit the Help screen.



4.2 Main

Use this menu for basic system configurations, such as time, date etc.



AMI BIOS, Processor, System Memory

These items show the firmware and hardware specifications of your system. Read only.

System Time

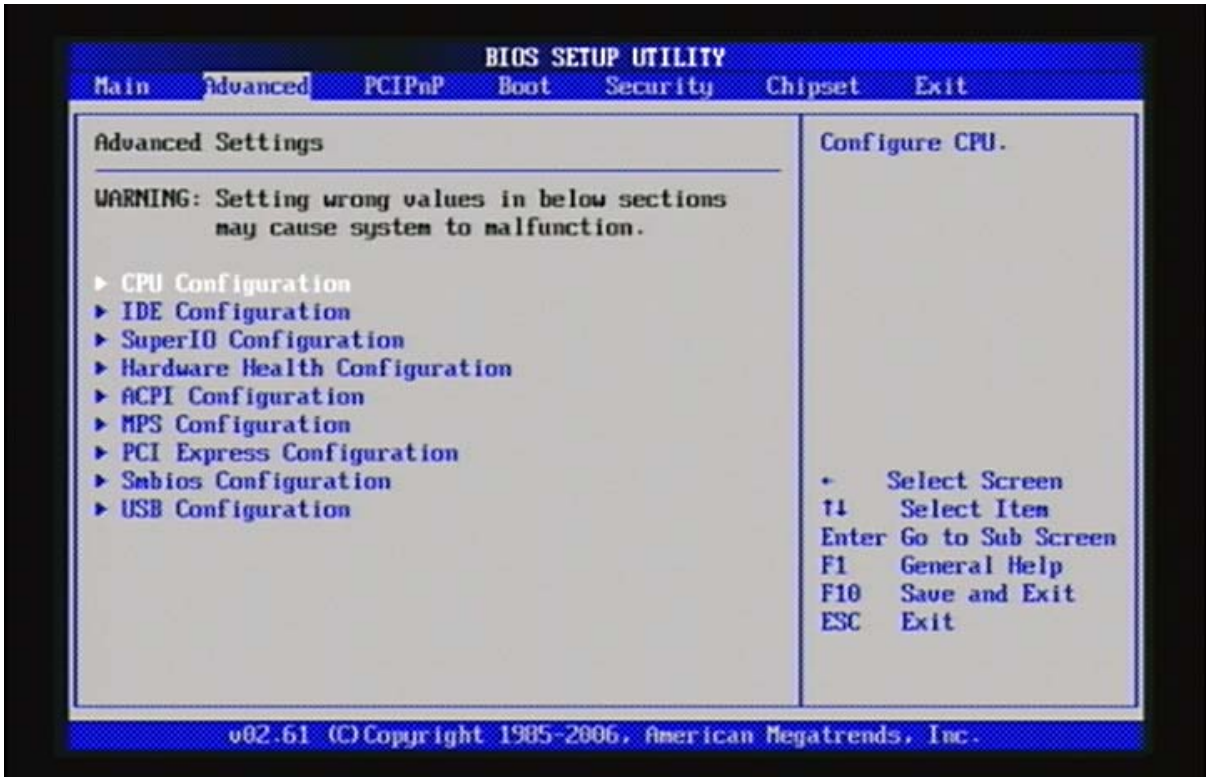
The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

System Date

The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

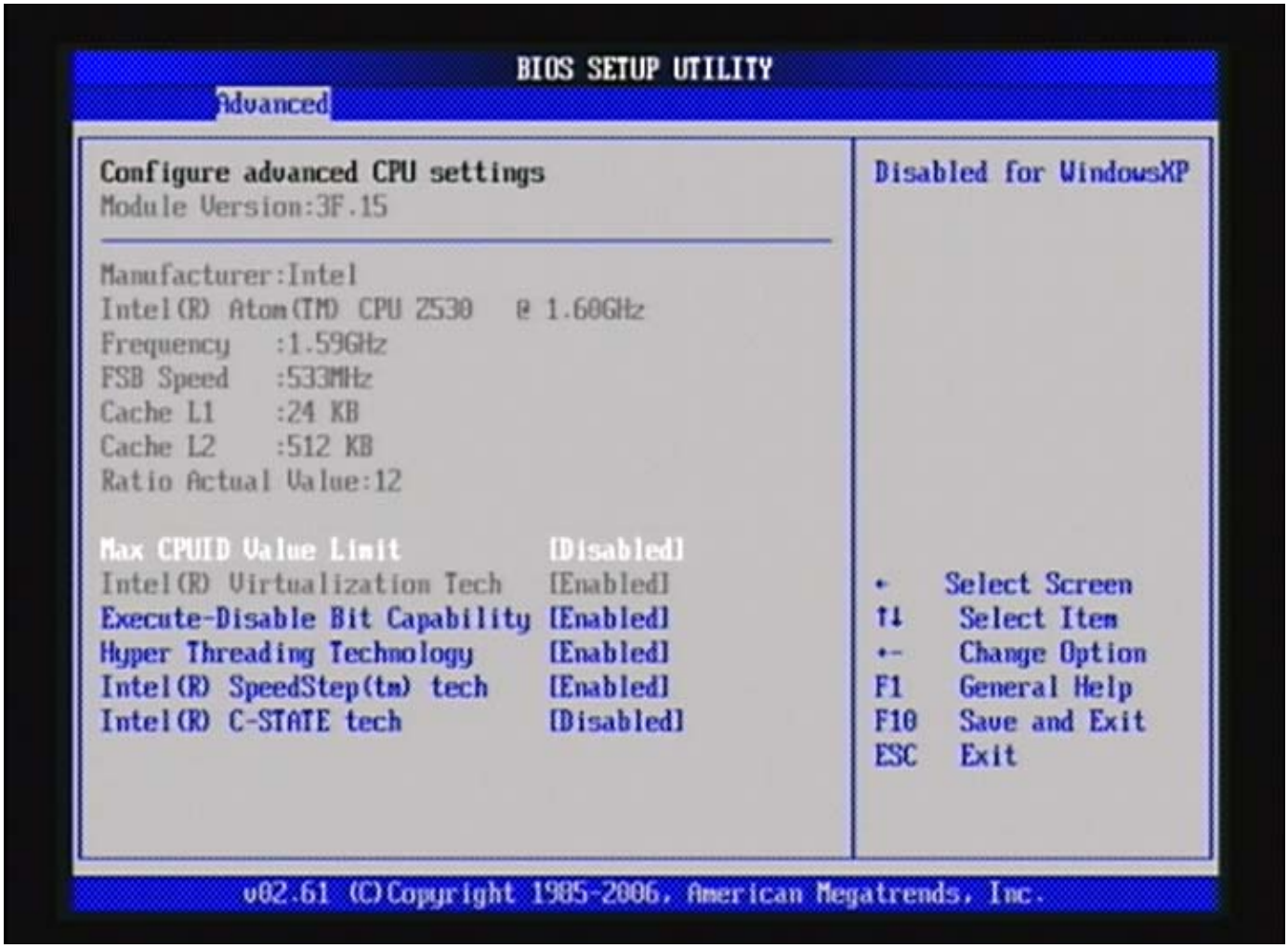
4.3 Advanced

Use this menu to set up the items of special enhanced features.



CPU Configuration

These items show the advanced specifications of your CPU. Read only.



Max CPUID Value Limit

Disabled for Windows XP

The choice: Disabled, Enabled.

Execute-Disable Bit capability

When disabled, force the XD feature flag to always return 0

The choice: Disabled, Enabled.

Hyper Threading Technology

Enable for Windows XP and Linux4 (OS optimized for Hyper Threading Technology) and disabled for other OS (OS not optimized for Hyper-Threading Technology)

Intel(R) Speed Step (tm) Tech

Disable: Disable GV3.
Enable: Enable GV3.

The choice: Disabled, Enabled.

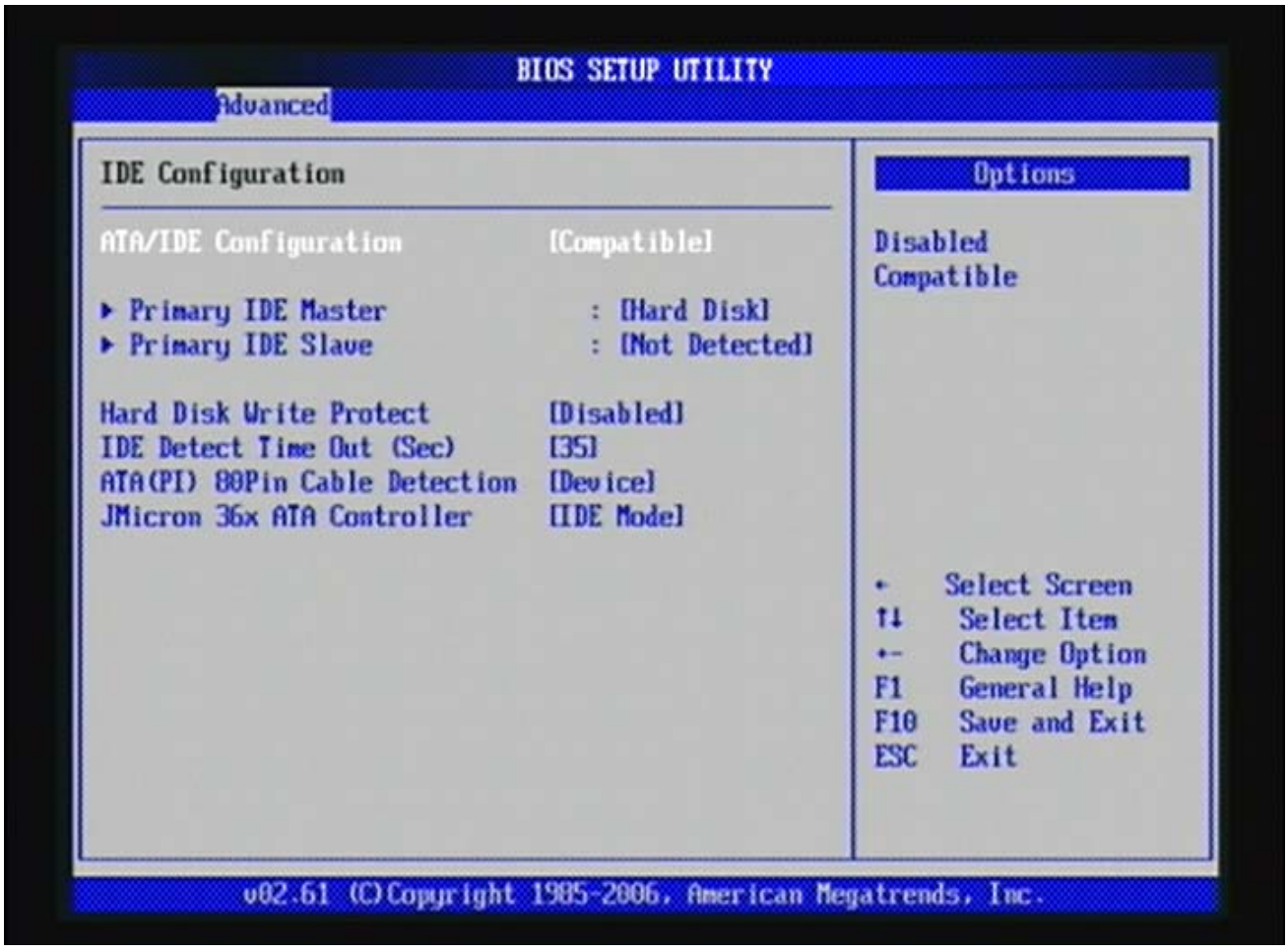
Intel(R) C-STATE Tech

CPU idle is set to C2, C3, C4 State.

The choice: Disabled, Enabled.

IDE Configuration

The IDE Configuration the IDE devices, such as hard disk drive or CD-ROM drive. It uses a separate sub menu to configure each hard disk drive (Master and Slave).

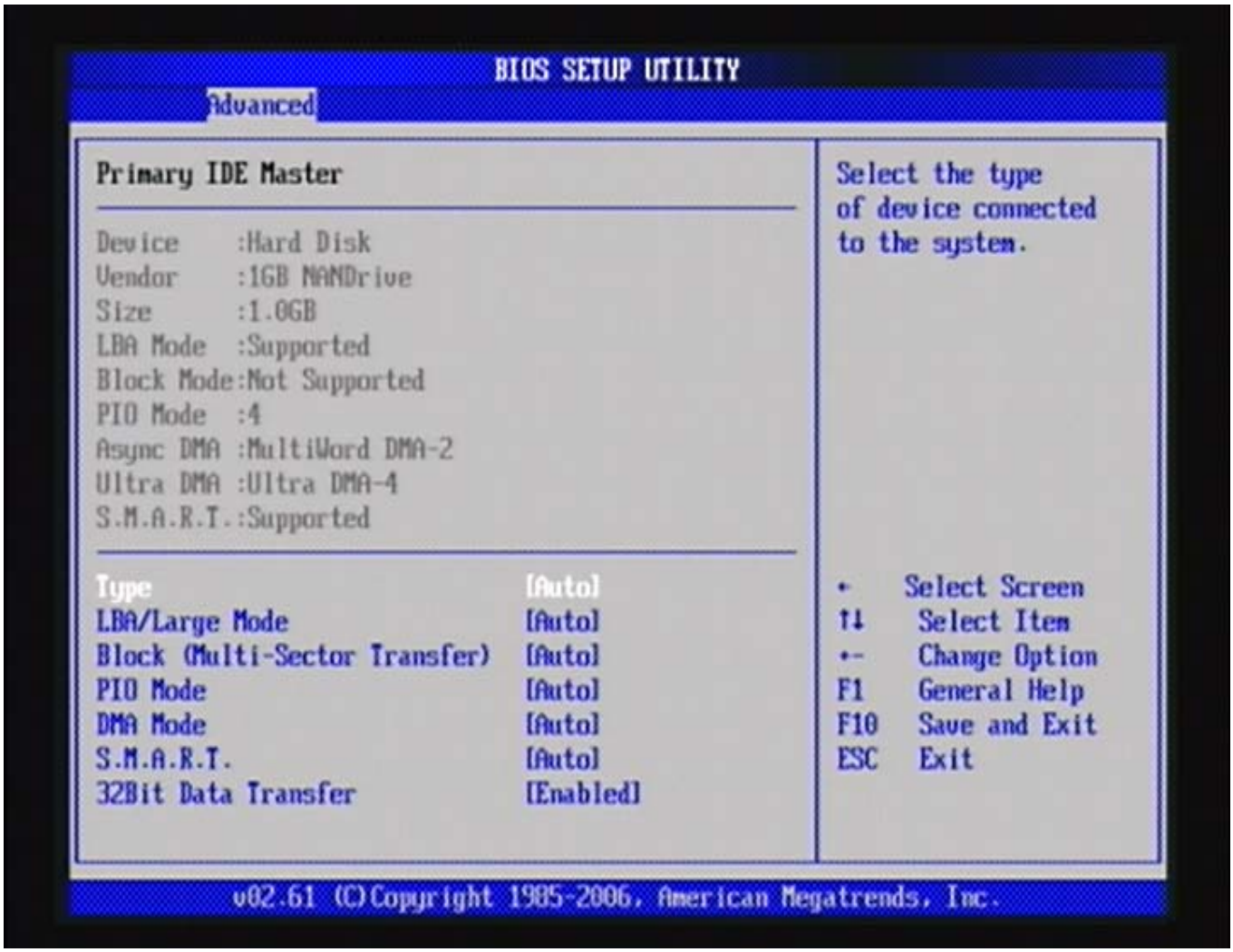


ATA/IDE Configuration

The choice: Disabled, Compatible.

Primary IDE Master/Slave

While entering setup, BIOS auto detects the presence of IDE devices. This display shows the status of auto detection of IDE devices.



[Type] Press PgUp/<+> or PgDn/<—> to select [Manual], [None] or [Auto] type. You can use [Manual] to define your own drive type manually.

[LBA/Large Mode] Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads and Sectors.

[Block (Multi-Sector Transfer)] Any selection except Disabled determines the number of sectors transferred per block.

[PIO Mode] Indicates the type of PIO (Programmed Input/Output)

[DMA Mode] Indicates the type of Ultra DMA

[S.M.A.R.T.] This allows you to activate the S.M.A.R.T. (Self-Monitoring Analysis & Reporting Technology) capability for the hard disks. S. M.A.R.T is a utility that monitors your disk status to predict hard disk failure. This gives you an opportunity to move data from a hard disk that is going to fail to a safe place before the hard disk becomes offline.

[32 Bit Data Transfer] Enable/Disable 32-bit Data Transfer.

Hard Disk Write Protect

Disabled/Enabled device write protection, this will be effective only if device is accessed through BIOS.

The choice: Disabled, Enabled.

IDE Detect Time Out (Sec)

Select the time out value for detecting ATA/ATAPI device (s).

The choice: 0, 5, 10, 15, 20, 25, 30, 35.

ATA(PI) 80Pin Cable Detection

Select the mechanism for detecting 80Pin ATA (PI) cable.

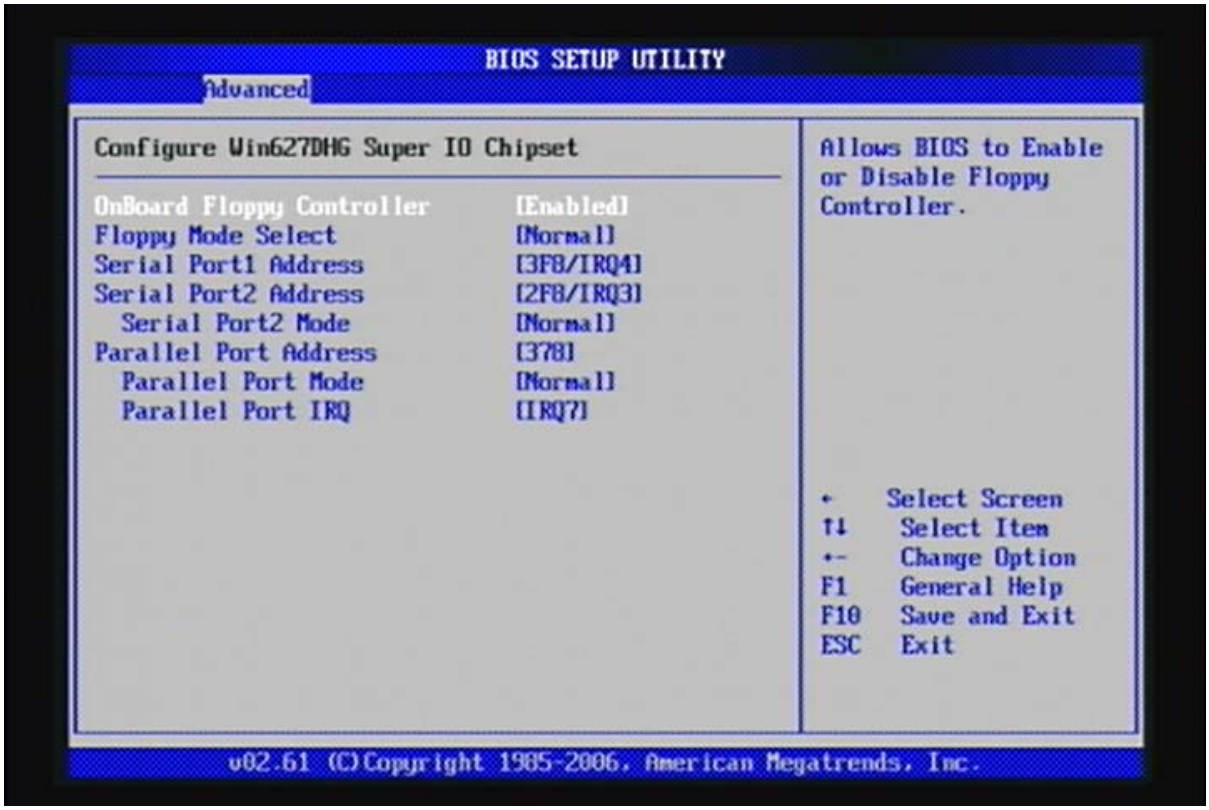
The choice: Host & Device, Host, Device.

JMicron 36x ATA Controller

Select ATA Controller Operate Mode

The choice: Disabled, IDE Mode, AHCI+IDE Mode.

Super IO Configuration



Onboard Floppy Controller

Allows BIOS to Enable or Disable Floppy controller.
The choice: Disabled, Enabled.

Floppy Mode Select

The choice: Normal, Write Protect

Serial Port 1 Address

Allows BIOS Select Serial Port1 Base Addresses.
The choice: Disabled, 3F8/IRQ4, 3E8/IRQ4, 2E8/IRQ3.

Serial Port 2 Address

Allows BIOS Select Serial Port2 Base Addresses.
The choice: Disabled, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3.

Serial Port 2 Mode

Allows BIOS Select mode for Serial Port2.
The choice: Normal, IrDA, ASK IR.

Parallel Port Address

Allows BIOS to Select Parallel Port Base Addresses.
The choice: Disabled, 378, 278, 3BC.

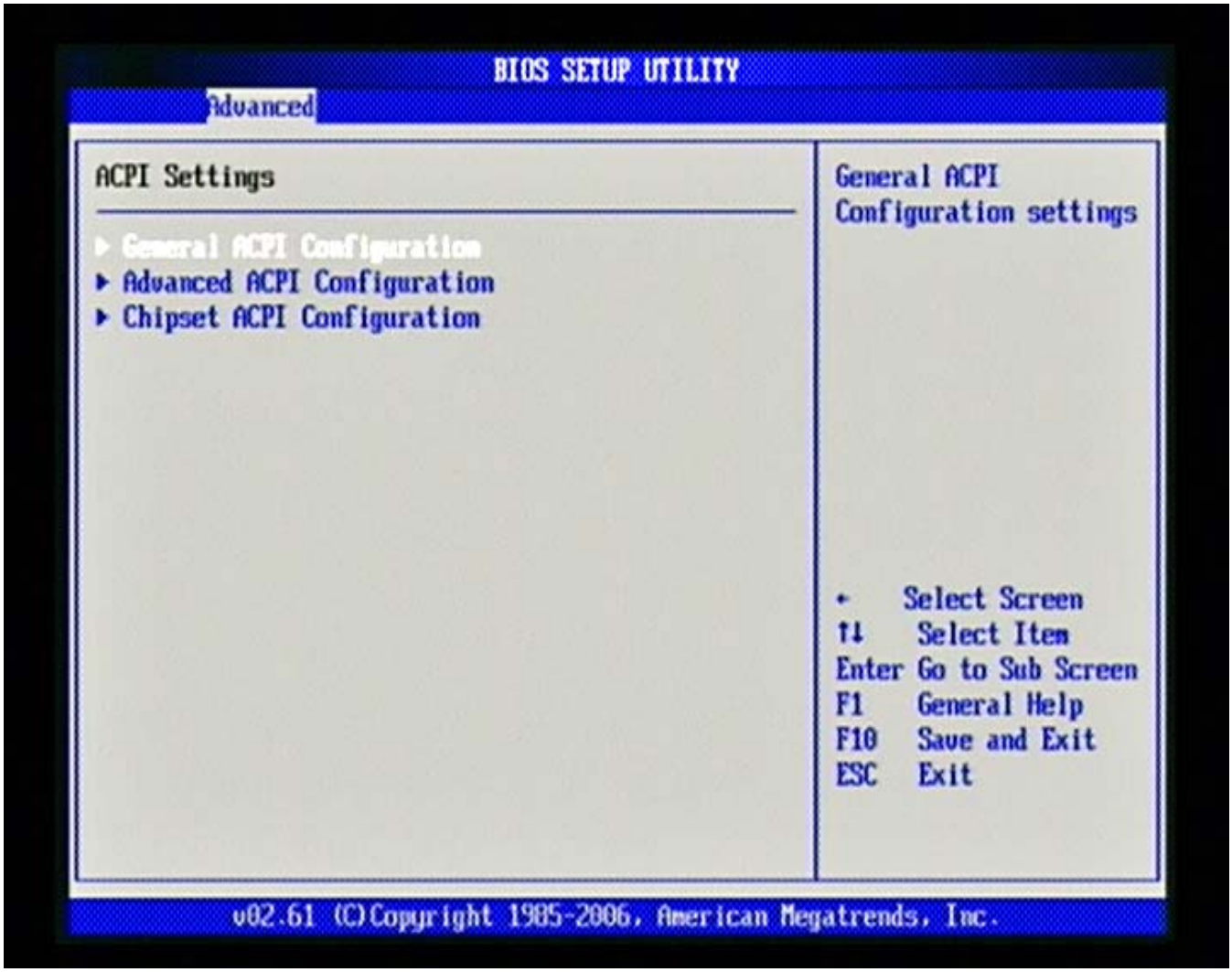
Parallel Port Mode

Allows BIOS to Select Parallel Port mode.
The choice: Normal, Bi-Directional, ECP, EPP, ECP &EPP.

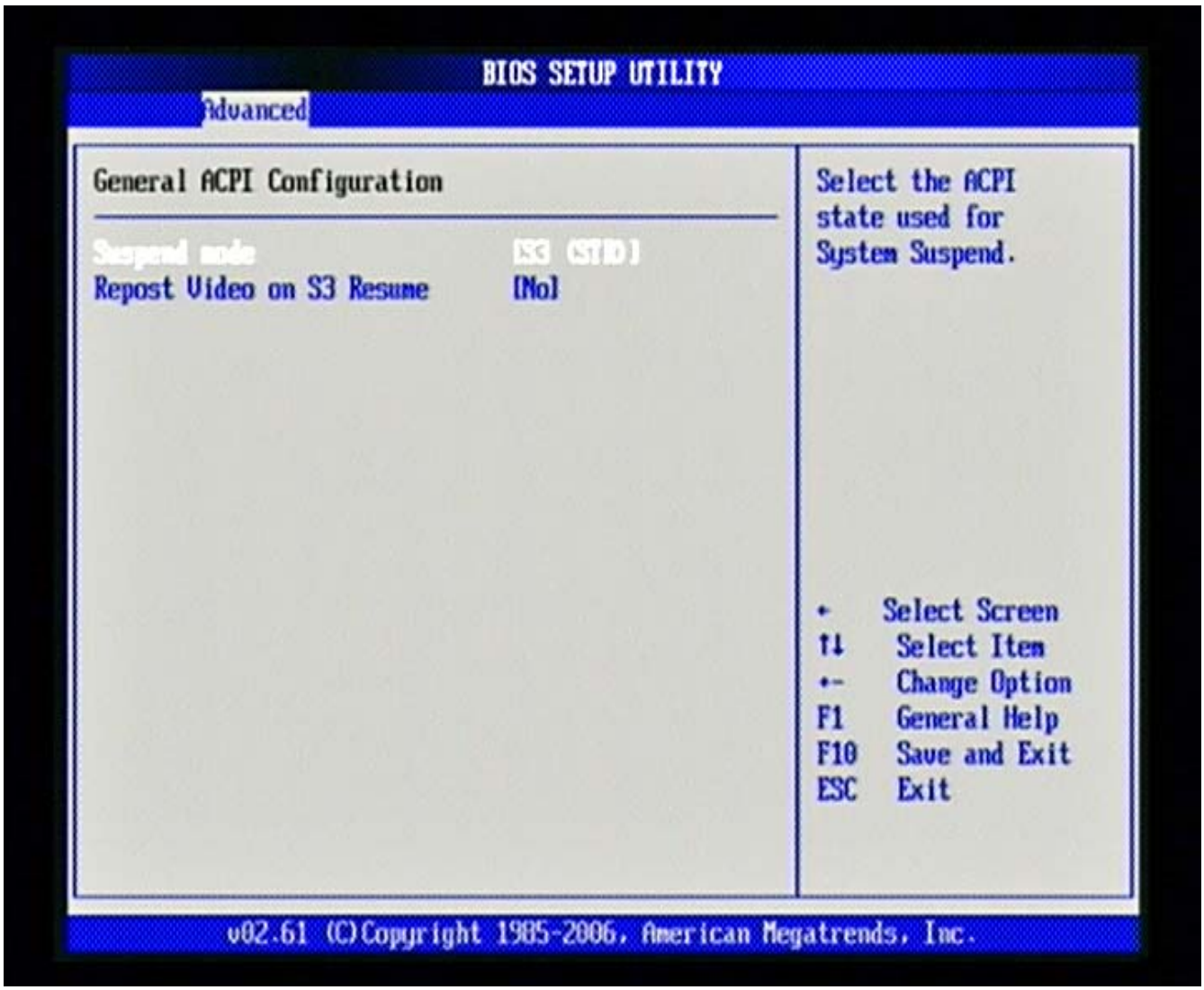
Parallel Port IRQ

Allows BIOS to Select Parallel Port IRQ.
The choice: IRQ5, IRQ7.

ACPI Settings



General ACPI Configuration



Suspend mode

Select the ACPI state used for System Suspend.

[S3 (STR)] The S3 sleep mode is a lower power state where the information of system configuration and open applications/ files is saved to main memory that remains powered while most other hardware components turn off to save energy. The information stored in memory will be used to restore the system when a "wake up" event occurs.

The choice: S3 (STR)

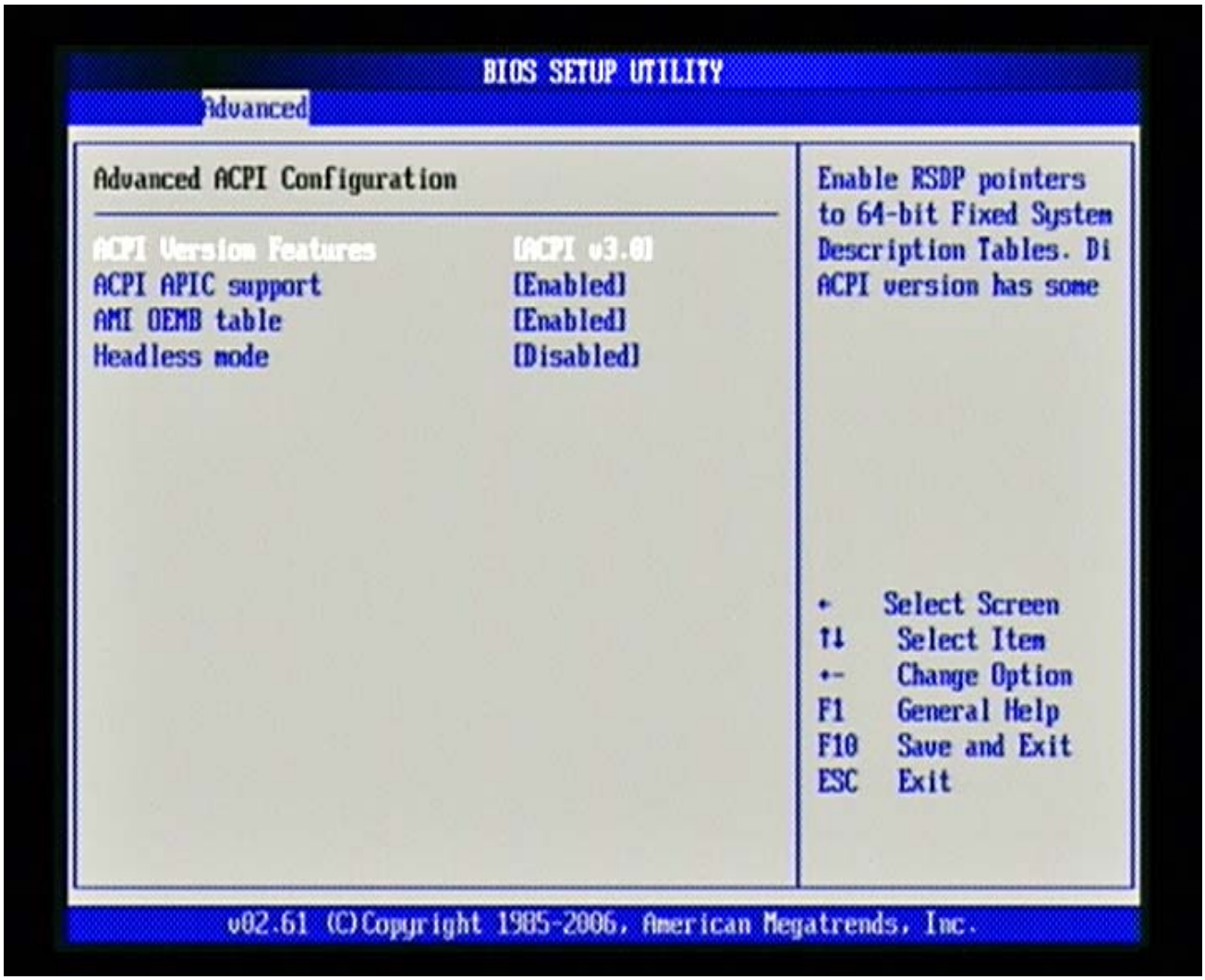
Repost Video on S3 Resume

Determines whether to invoke VGA BIOS post on S3/STR resume.

The choice: No, Yes

Advanced ACPI Configuration

Advanced ACPI Configuration settings, Use this section to configure additional ACPI options.


BIOS SETUP UTILITY
Advanced
Advanced ACPI Configuration
ACPI Version Features [ACPI v3.0]
ACPI APIC support [Enabled]
AMI OEMB table [Enabled]
Headless mode [Disabled]
Enable RSDP pointers to 64-bit Fixed System Description Tables. Di ACPI version has some
→ Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
v02.61 (C)Copyright 1985-2006, American Megatrends, Inc.

ACPI Version Features

Enable RSDP pointers to 64-bit Fixed System Description Tables.

The choice: ACPI v1.0 / ACPI v2.0 / ACPI v3.0.

ACPI APIC support

Include ACPI APIC table pointer to RSDT pointer list.

The choice: Disabled, Enabled.

AMI OEMB table

Include OEMB table pointer to R(X) SDT pointer list.

The choice: Disabled, Enabled.

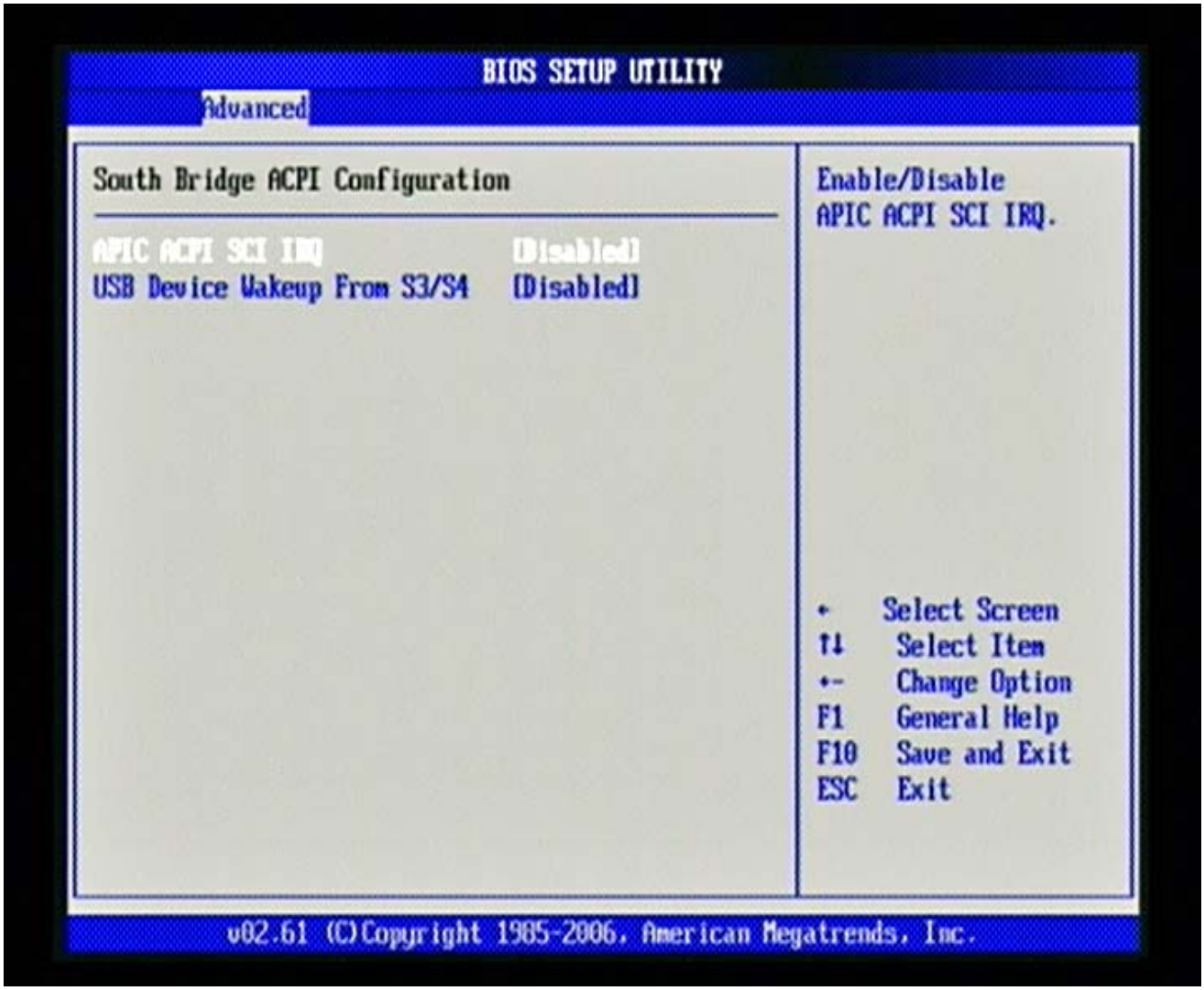
Headless mode

Enable / Disable Headless operation mode through ACPI.

The choice: Disabled, Enabled.

South Bridge ACPI Configuration

The South Bridge ACPI related Configuration settings, Use this section to configure additional ACPI options.



APIC ACPI SCI IRQ

Enable / Disable APIC ACPI SCI IRQ.

The choice: Disabled, Enabled.

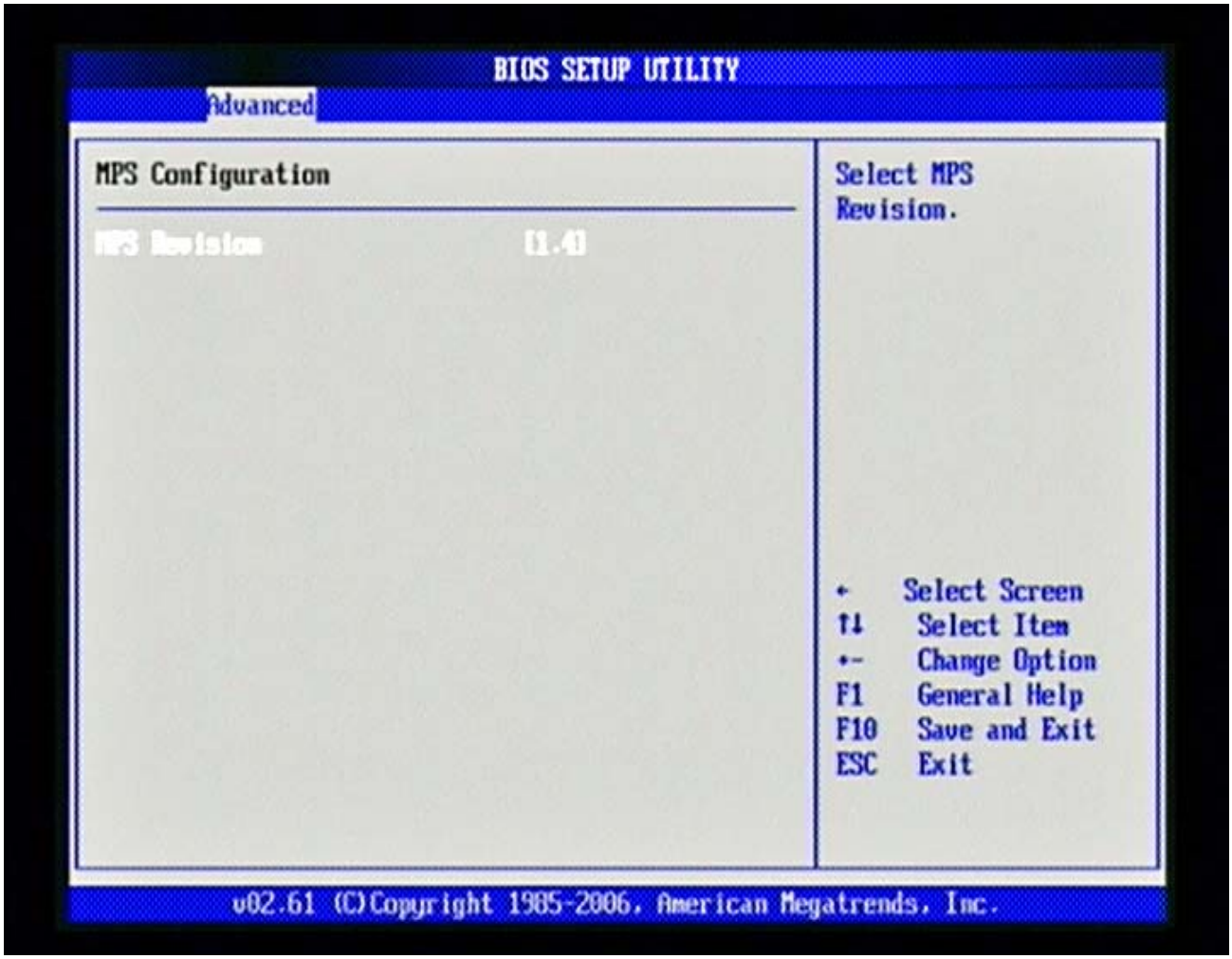
USB Device Wakeup From S3/S4

Enable / Disable USB device Wake from S3/S4 mode.

The choice: Disabled, Enabled.

MPS Configuration

Configure the Multi-Processor Table.



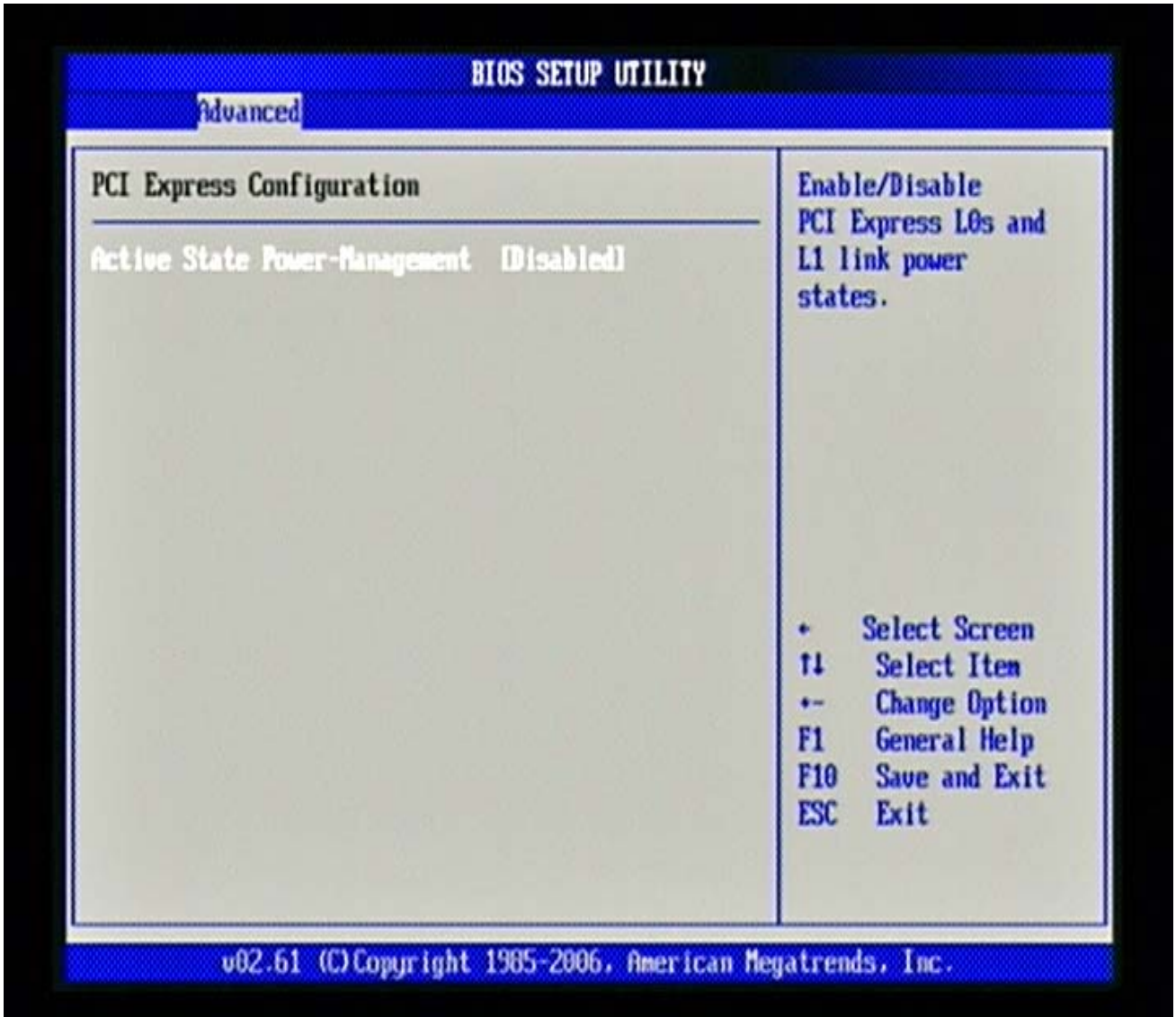
MPS Revision

This field allows you to select which MPS (Multi-Processor Specification) version to be used for the operating system. You need to select the MPS version supported by your operating system. To find out which version to use, consult the vendor of your operating system.

The choice: 1.1, 1.4.

PCI Express Configuration

PCI Express Configuration Menu



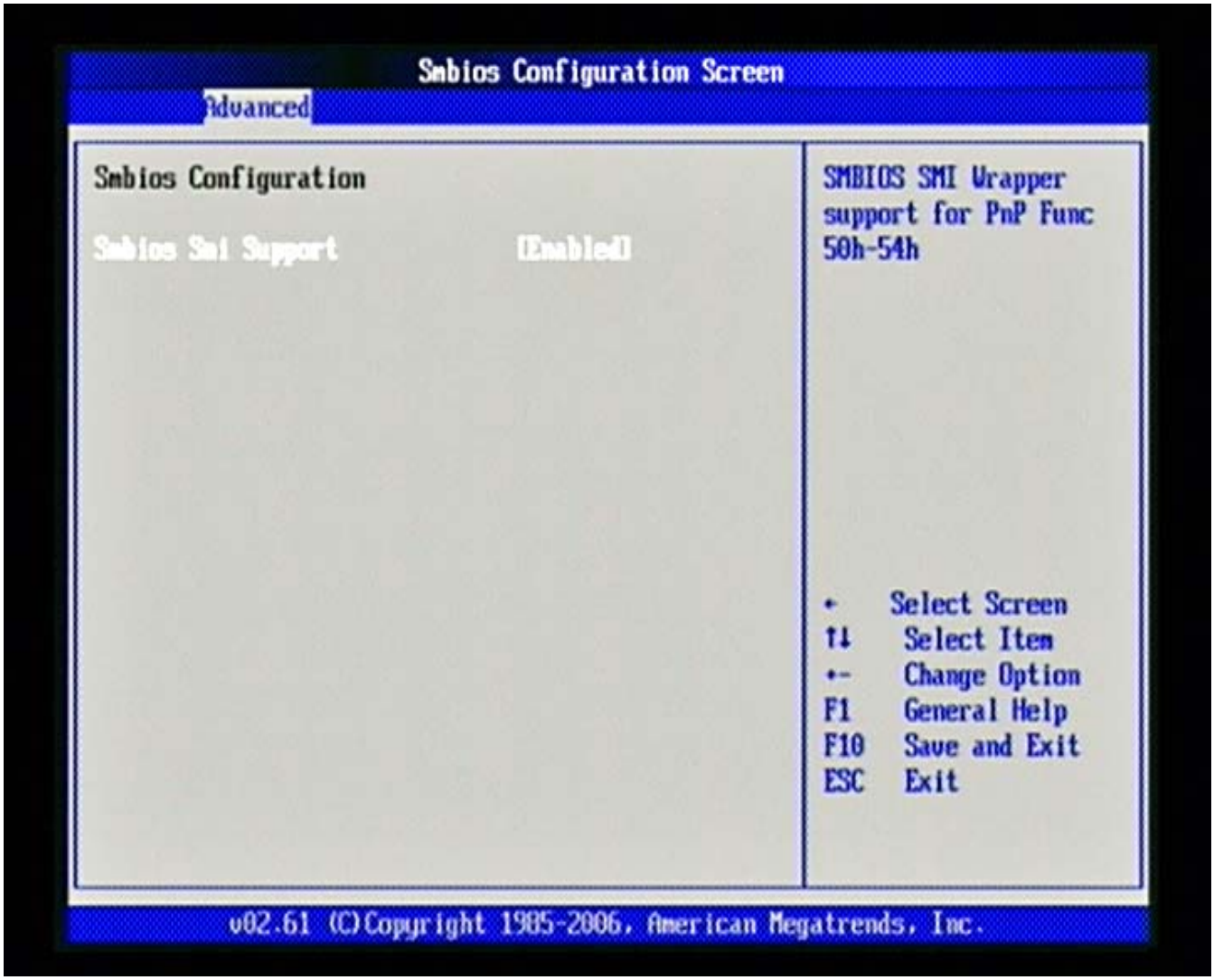
Active State Power-Management

Enable/Disable PCI Express L0s and L1 link power states.

The choice: Disabled, Enabled.

Smbios Configuration

SMBIOS Configuration Menu

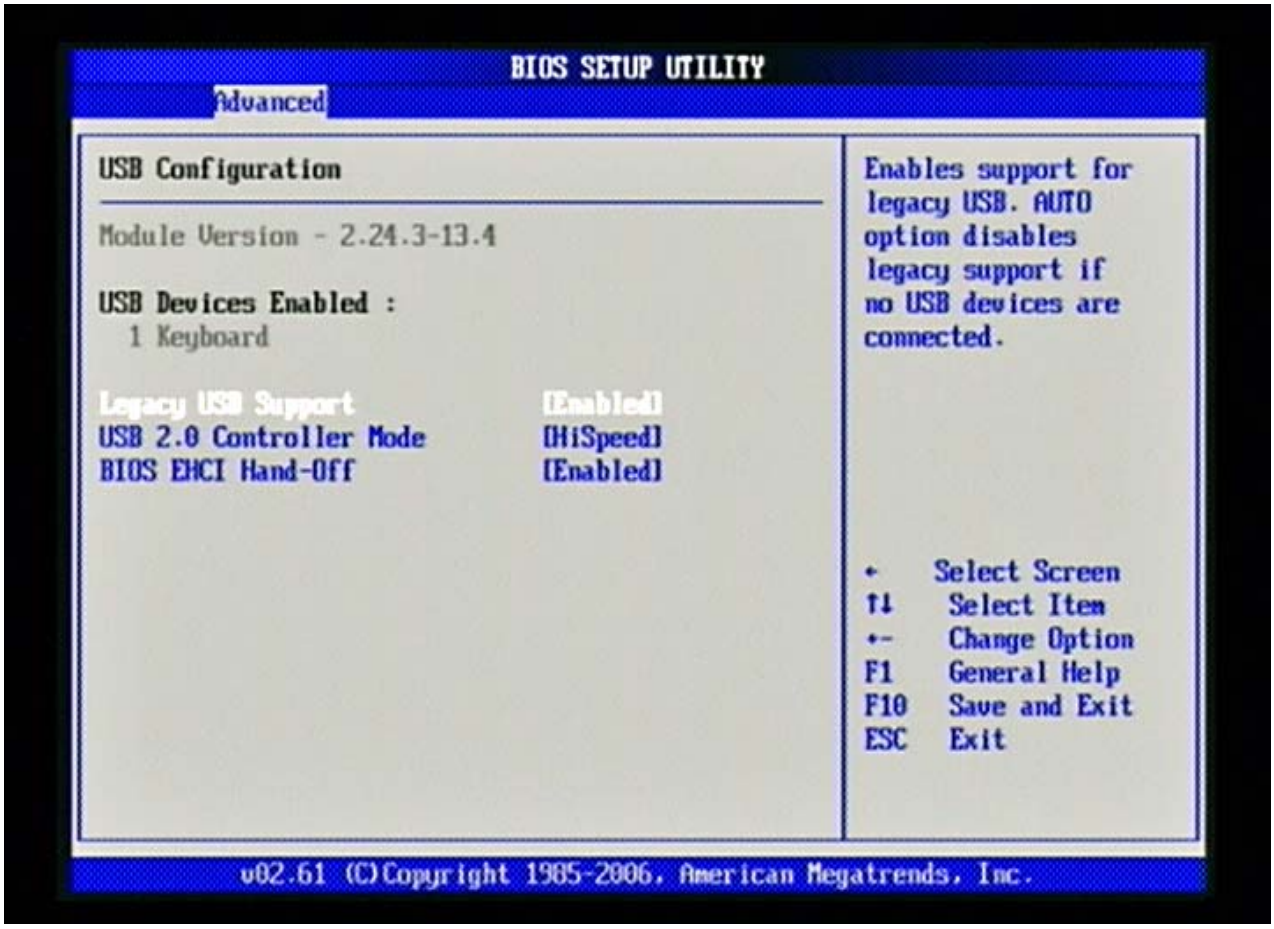


Smbios Smi Support

SMBIOS SMI Wrapper support for PnP Function 50h-54h

The choice: Disabled, Enabled.

USB Configuration


BIOS SETUP UTILITY
Advanced
USB Configuration
Module Version - 2.24.3-13.4
USB Devices Enabled :
1 Keyboard
Legacy USB Support [Enabled]
USB 2.0 Controller Mode [HiSpeed]
BIOS EHCI Hand-Off [Enabled]
Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected.
← Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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Legacy USB Support

Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected.

The choice: Disabled, Enabled, Auto.

USB 2.0 Controller Mode

Configures the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps).

The choice: FullSpeed, HiSpeed.

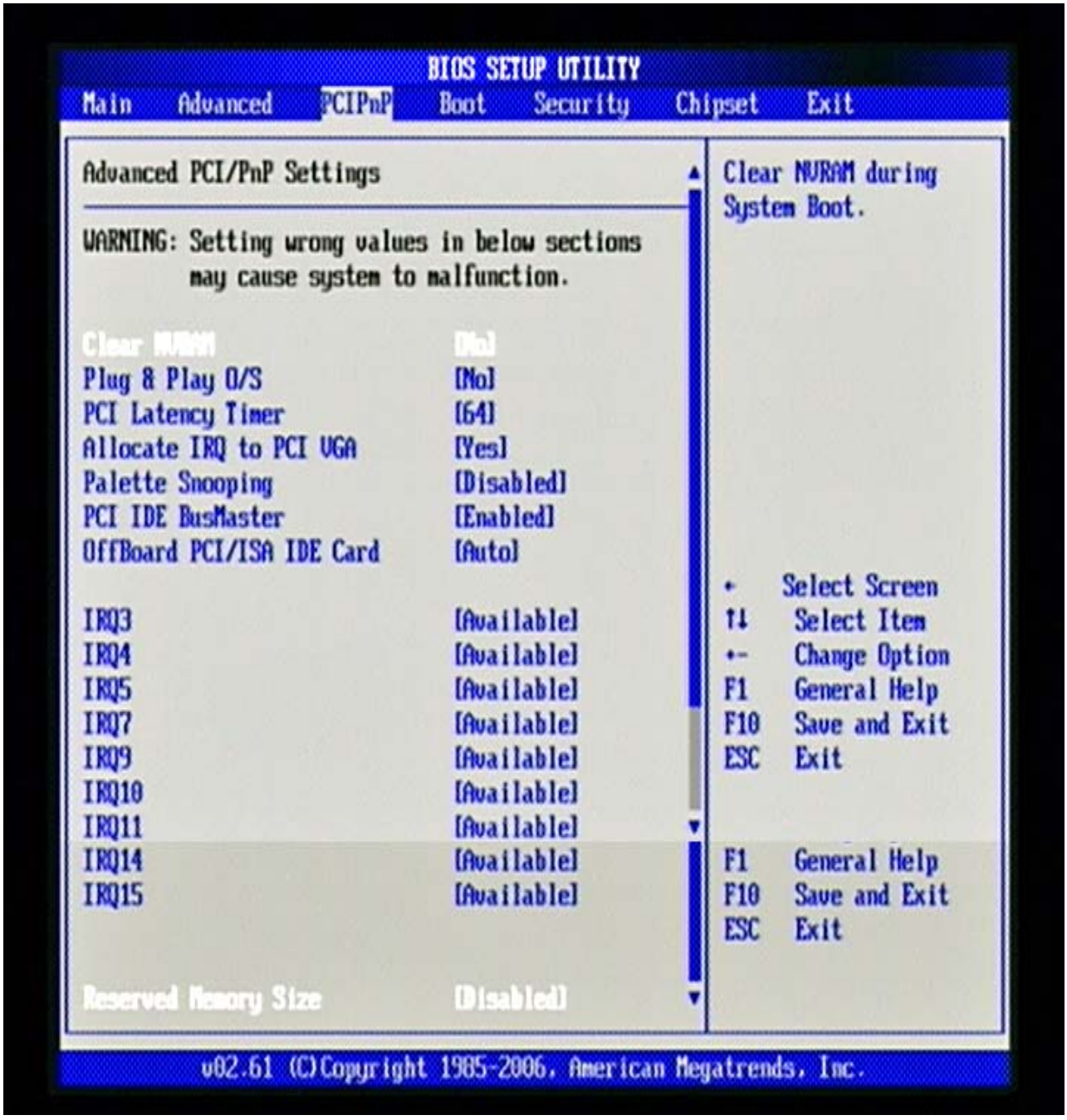
BIOS EHCI Hand-Off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

The choice: Disabled, Enabled.

4.4 PCIPnP

Advanced PCI/PnP setting wrong values in below sections may cause system to malfunction.



Clear NVRAM

Clear NVRAM during System Boot.

The choice: No, Yes.

Plug & Play O/S

No: lets the BIOS configure all the devices in the system.
Yes: lets the operating system configure Plug and Play (PnP) devices not required for boot if your system has a Plug and Play operating system.

The choice: No, Yes.

PCI Latency Timer

Select value in units of PCI clocks for PCI device latency timer register.

The choice: 32, 64, 96, 128, 160, 192, 224, 248.

Allocate IRQ to PCI VGA

Yes: Assigns IRQ to PCI VGA card if card requests IRQ.
No: Does not assign IRQ to PCI VGA card if card requests an IRQ.
The choice: Yes, No.

Palette Snooping

Enabled: Informs the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.

The choice: Disabled, Enabled.

PCI IDE BusMaster

Enabled: BIOS Uses PCI busmastering for reading / writing to IDE drives.

The choice: Disabled, Enabled.

OffBoard PCI/ISA IDE Card

Some PCI IDE cards may require this to be set to the PCI slot number that is holding the card.

AUTO: Works for most PCI IDE cards

The choice: Auto, PCI Slot1, PCI Slot2, PCI Slot3, PCI Slot4, PCI Slot5, PCI Slot6.

IRQ 3 / IRQ 4 / IRQ5 / IRQ7 / IRQ 9 / IRQ 10 / IRQ 11 / IRQ 14 / IRQ 15

Available: Specified IRQ is available to be used by PCI/PnP devices.
Reserved: Specified IRQ is reserved for used by Legacy ISA devices.

The choice: Available, Reserved.

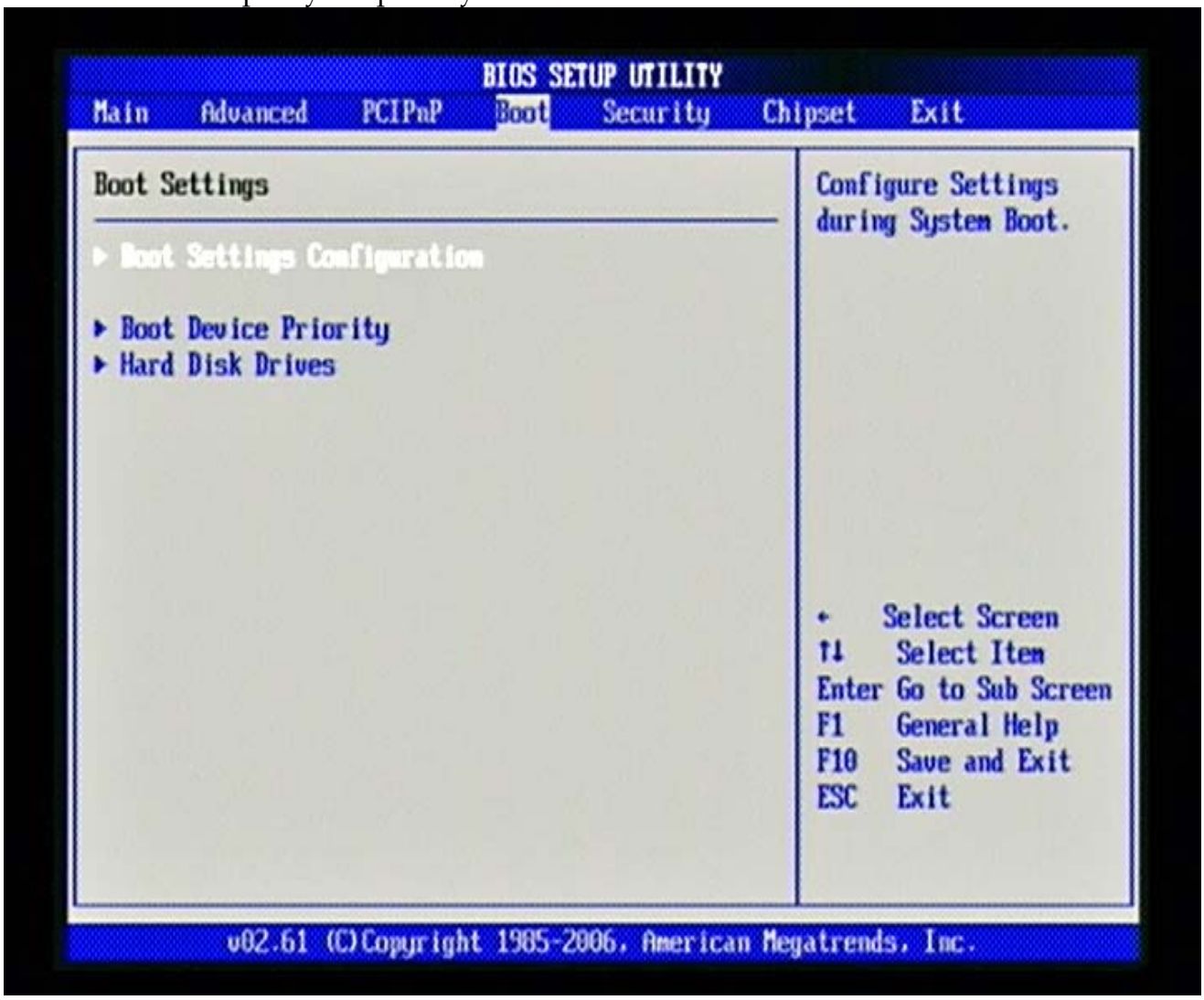
Reserved Memory Size

Select Size of memory block to reserve for legacy ISA devices.

The choice: Disabled, 16K, 32K, 64K.

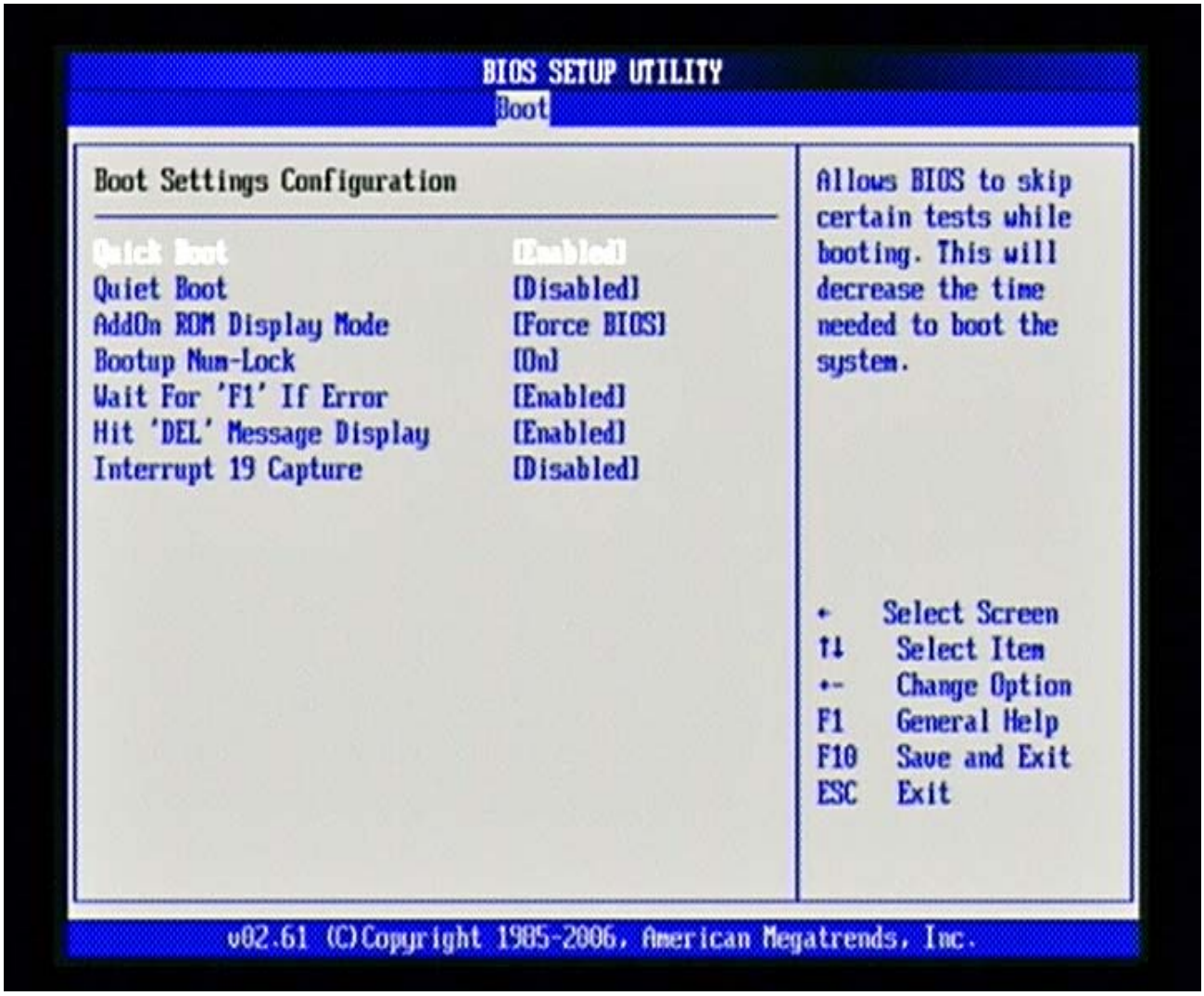
4.5 Boot

Use this menu to specify the priority of boot devices.



Boot Settings Configuration

Configure Settings during System Boot.


BIOS SETUP UTILITY
Boot
Boot Settings Configuration
Quick Boot [Enabled]
Quiet Boot [Disabled]
AddOn ROM Display Mode [Force BIOS]
Bootup Num-Lock [On]
Wait For 'F1' If Error [Enabled]
Hit 'DEL' Message Display [Enabled]
Interrupt 19 Capture [Disabled]
Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.
→ Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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Quick Boot

Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.

The choice: Disabled, Enabled.

Quiet Boot

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo. When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.

Disabled: Displays normal POST messages.
Enabled: Displays OEM Logo instead of POST messages.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

The choice: Disabled, Enabled.

AddOn ROM Display Mode

Set display mode for Option ROM.
This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

The choice: Force BIOS, Keep Current.

Bootup Num-Lock

Select Power-on state for Numlock.
Setting to [On] will turn on the Num Lock key when the system is powered on.
Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

The choice: Off, On.

Wait For 'F1' If Error

Wait for F1 key to be pressed if error occurs.
When this setting is set to [Enabled] and the boot sequence encounters an error, it asks you to press F1. If disabled, the system continues to boot without waiting for you to press any keys.

The choice: Disabled, Enabled.

Hit 'DEL' Message Display

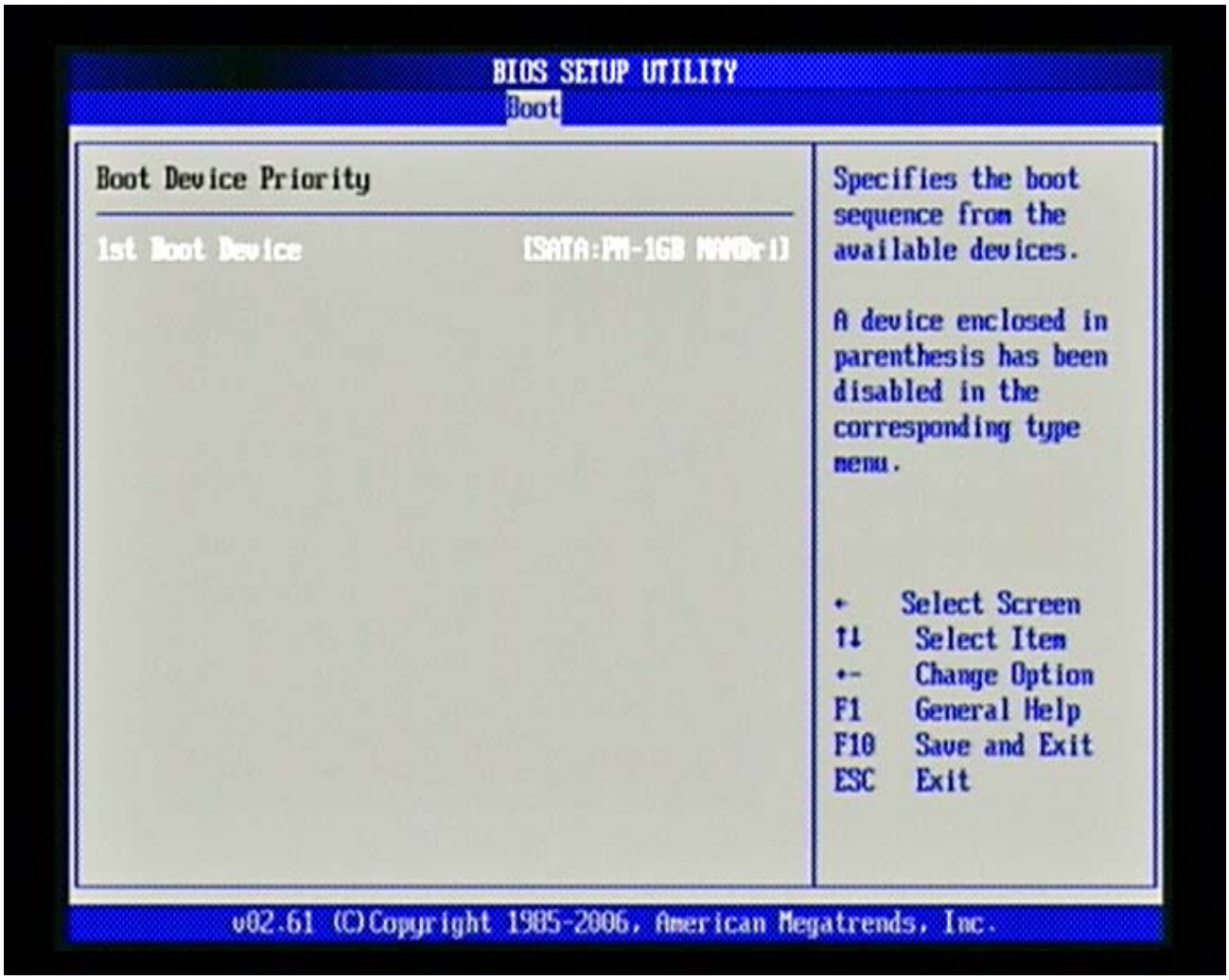
Displays "Press Del to run Setup" in POST.
The choice: Disabled, Enabled.

Interrupt 19 Capture

Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the ROM BIOS of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's ROM setup utility, if one is available.
When disabled, the ROM BIOS of these host adaptors will not be able to "cap ture" Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their ROM setup utilities.

The choice: Disabled, Enabled.

Boot Device Priority


BIOS SETUP UTILITY
Boot
Boot Device Priority
1st Boot Device
Specifies the boot sequence from the available devices.
A device enclosed in parenthesis has been disabled in the corresponding type menu.
Select Screen
Select Item
Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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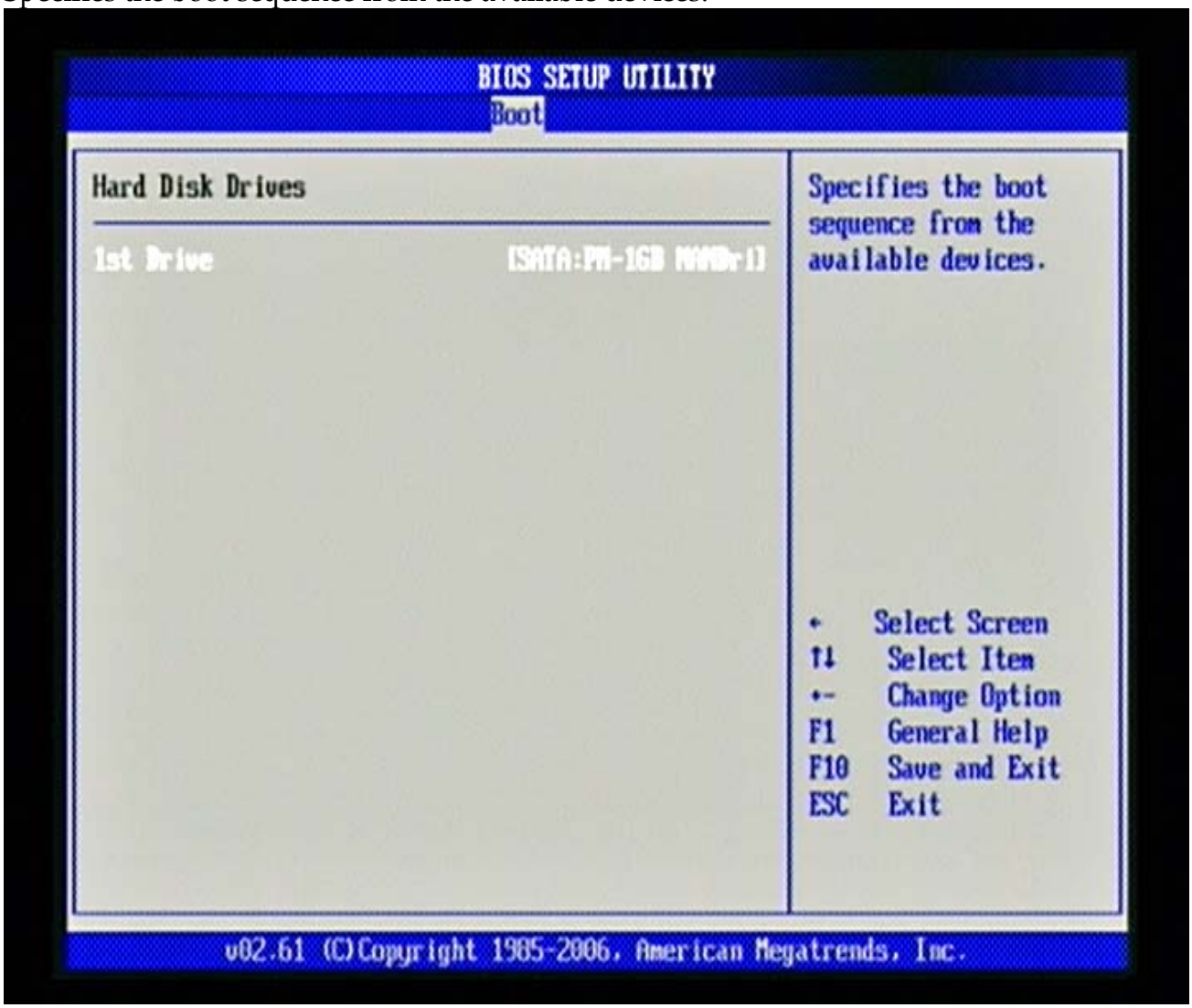
1st Boot Device

The items allow you to set the sequence of boot devices where BIOS attempts to load the disk operating system. First press <Enter> to enter the sub-menu. Then you may use the arrow keys (↑ ↓) to select the desired device, then press <+>, <—> or <PageUp>, <PageDown> key to move it up/down in the priority list.

The choice: (SATA: PM-1GB NANDrive), Disabled.

Hard Disk Drives

Specifies the boot sequence from the available devices.

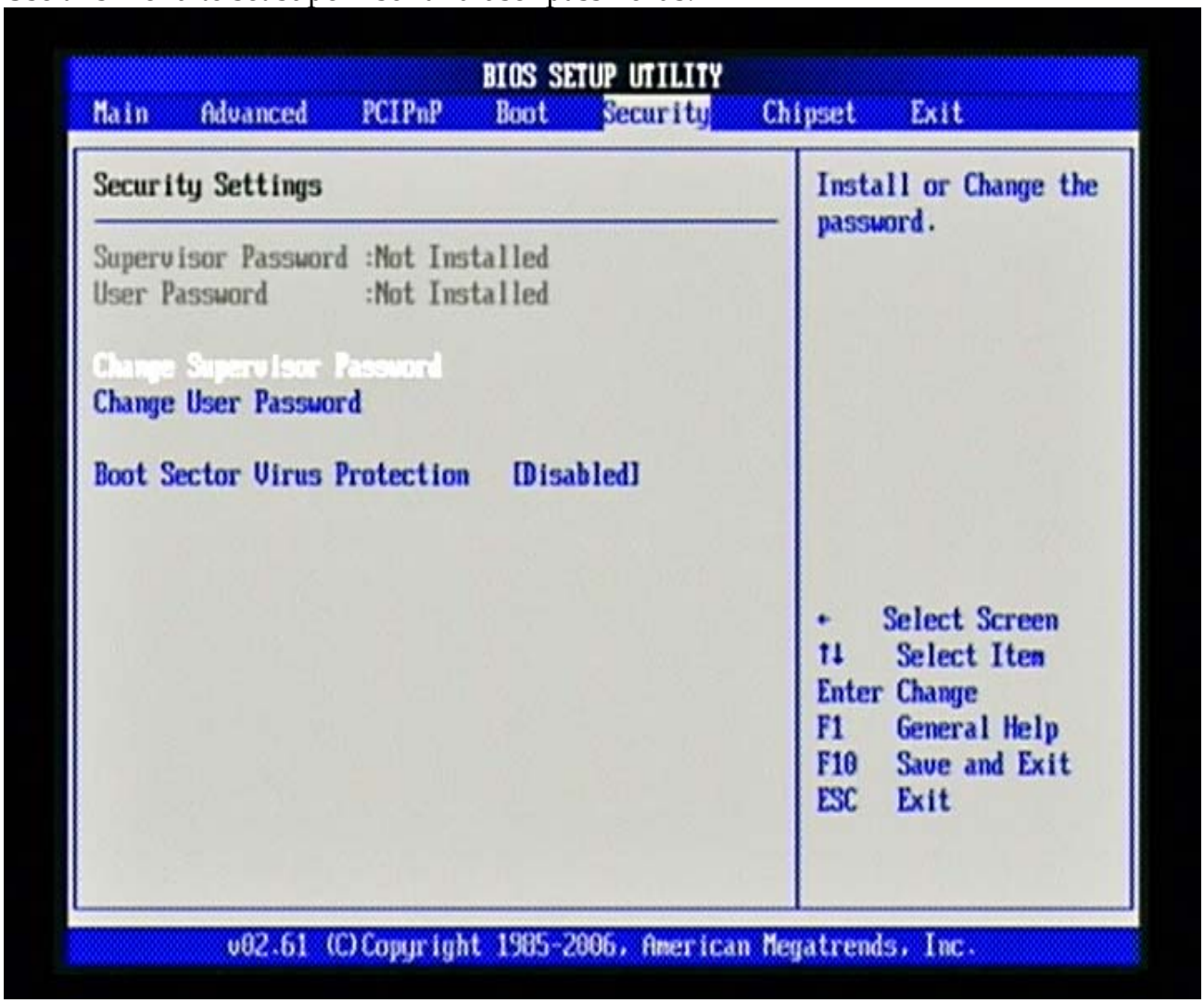


1st Drive

The choice: (SATA: PM-1GB NANDrive), Disabled.

4.6 Security

Use this menu to set supervisor and user passwords.



Supervisor Password / Change Supervisor Password

Supervisor Password controls access to the BIOS Setup utility. These settings allow you to set or change the supervisor password.

User Password / Change User Password

User Password controls access to the system at boot. These settings allow you to set or change the user password.

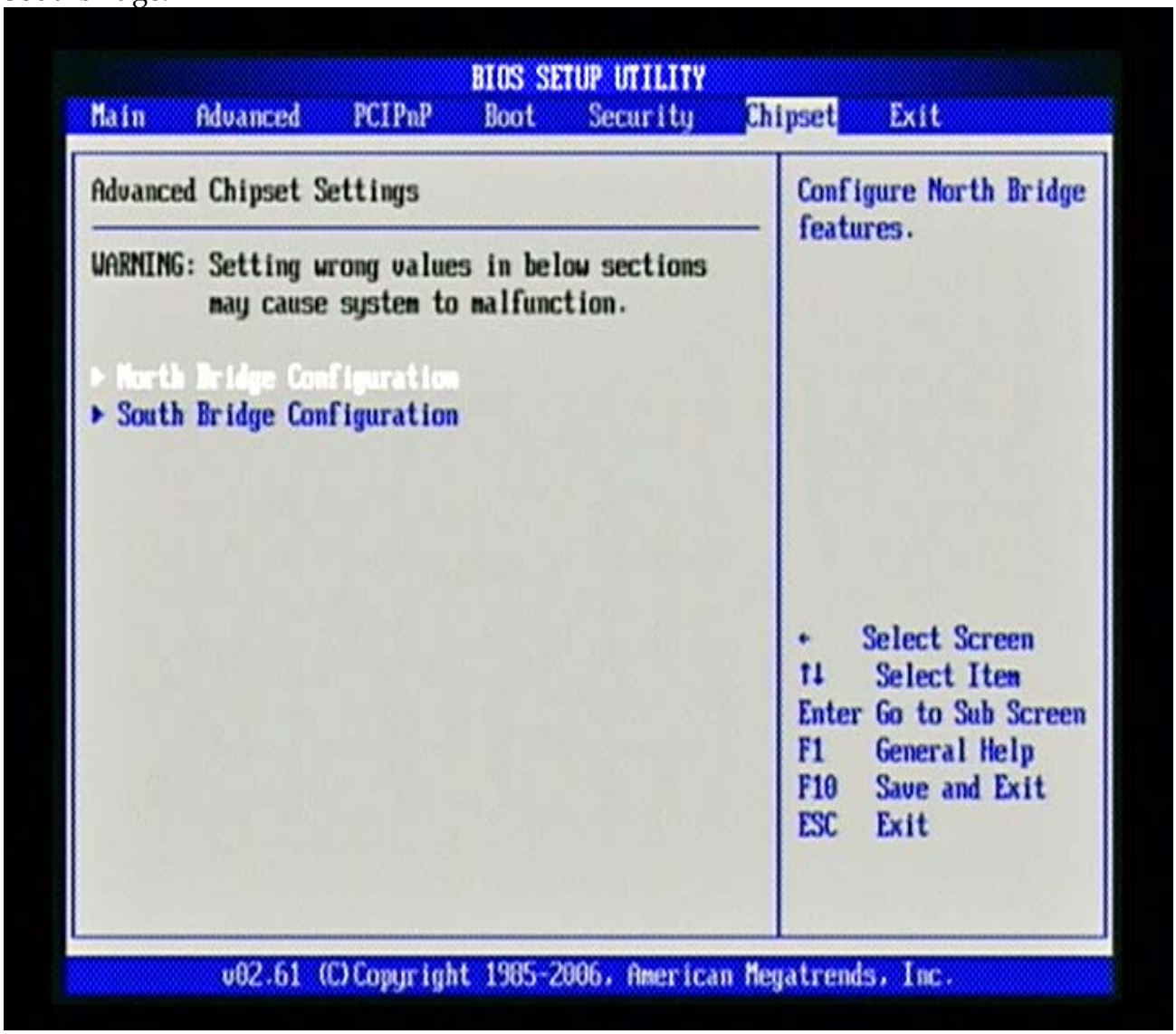
Boot Sector Virus Protection

Enable/Disable Boot Sector Virus Protection.

The choice: Disabled, Enabled.

4.7 Chipset

This menu controls the advanced features of the onboard Northbridge and Southbridge.


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Advanced Chipset Settings
WARNING: Setting wrong values in below sections may cause system to malfunction.
North Bridge Configuration
South Bridge Configuration
Configure North Bridge features.
Select Screen
Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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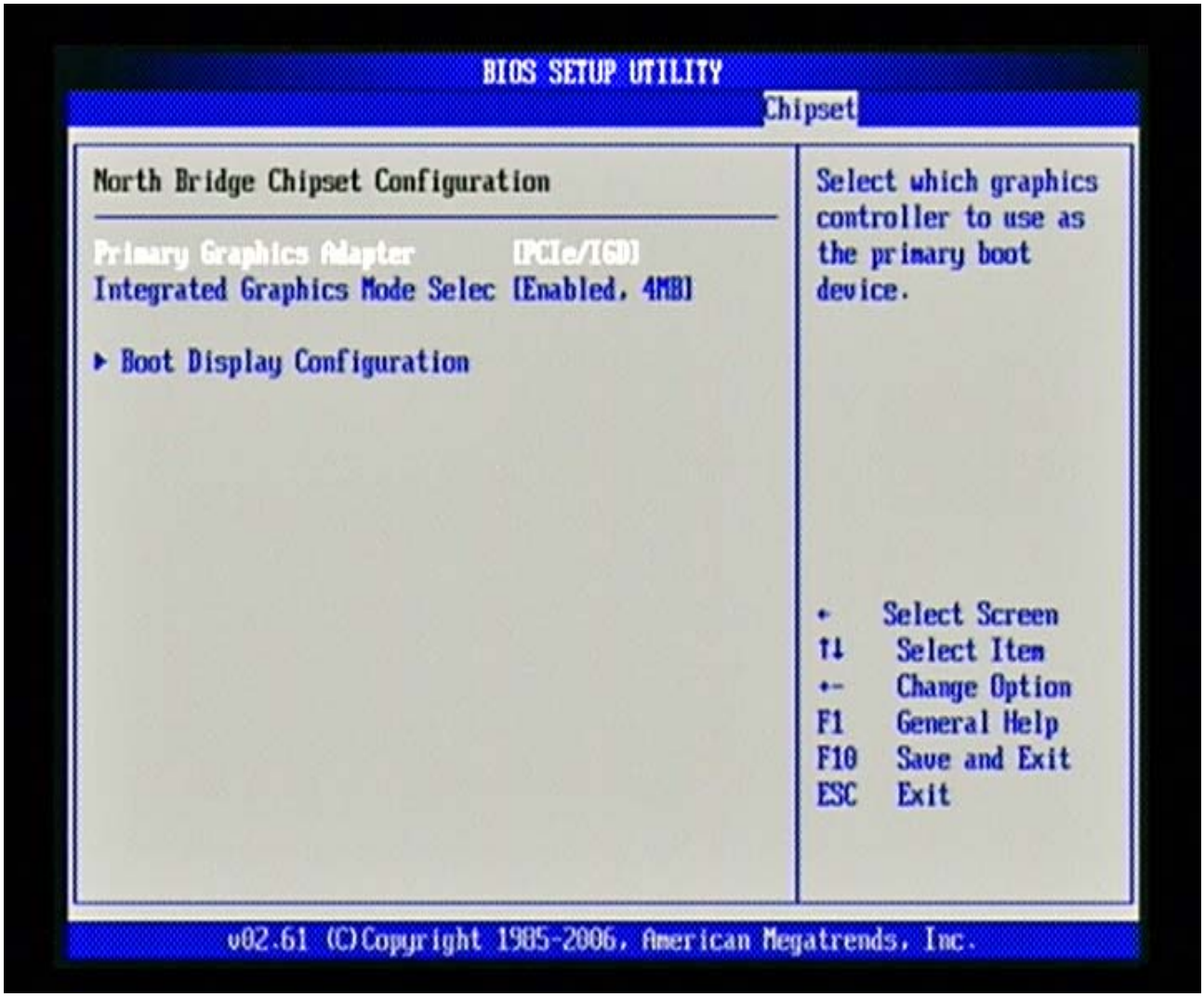
North Bridge Chipset Configuration


BIOS SETUP UTILITY
Chipset
North Bridge Chipset Configuration
Primary Graphics Adapter [PCIe/IGD]
Integrated Graphics Mode Selec [Enabled, 4MB]
▶ Boot Display Configuration
Select which graphics controller to use as the primary boot device.
↔ Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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Primary Graphics Adapter

Select which graphics controller to use as the primary boot device.

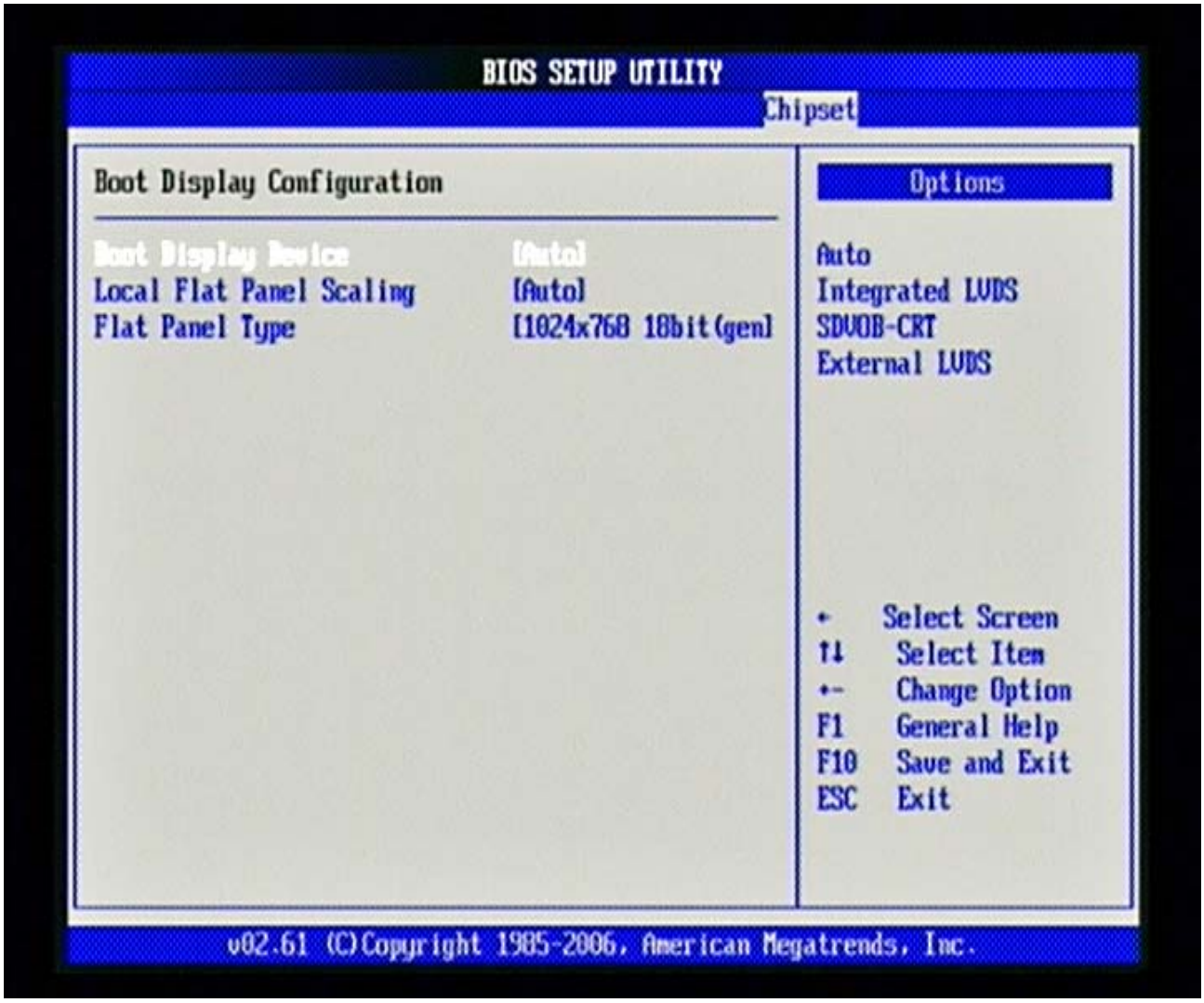
The choice: IGD, PCIe/IGD.

Integrated Graphics Mode Selec

Select the amount of system memory used by the internal graphics device.

The choice: Disabled, Enabled, 1MB, Enabled, 4MB, Enabled, 8MB.

Boot Display Configuration



Boot Display Device

The choice: Auto, Integrated LVDS, SDVOB-CRT, External LVDS.

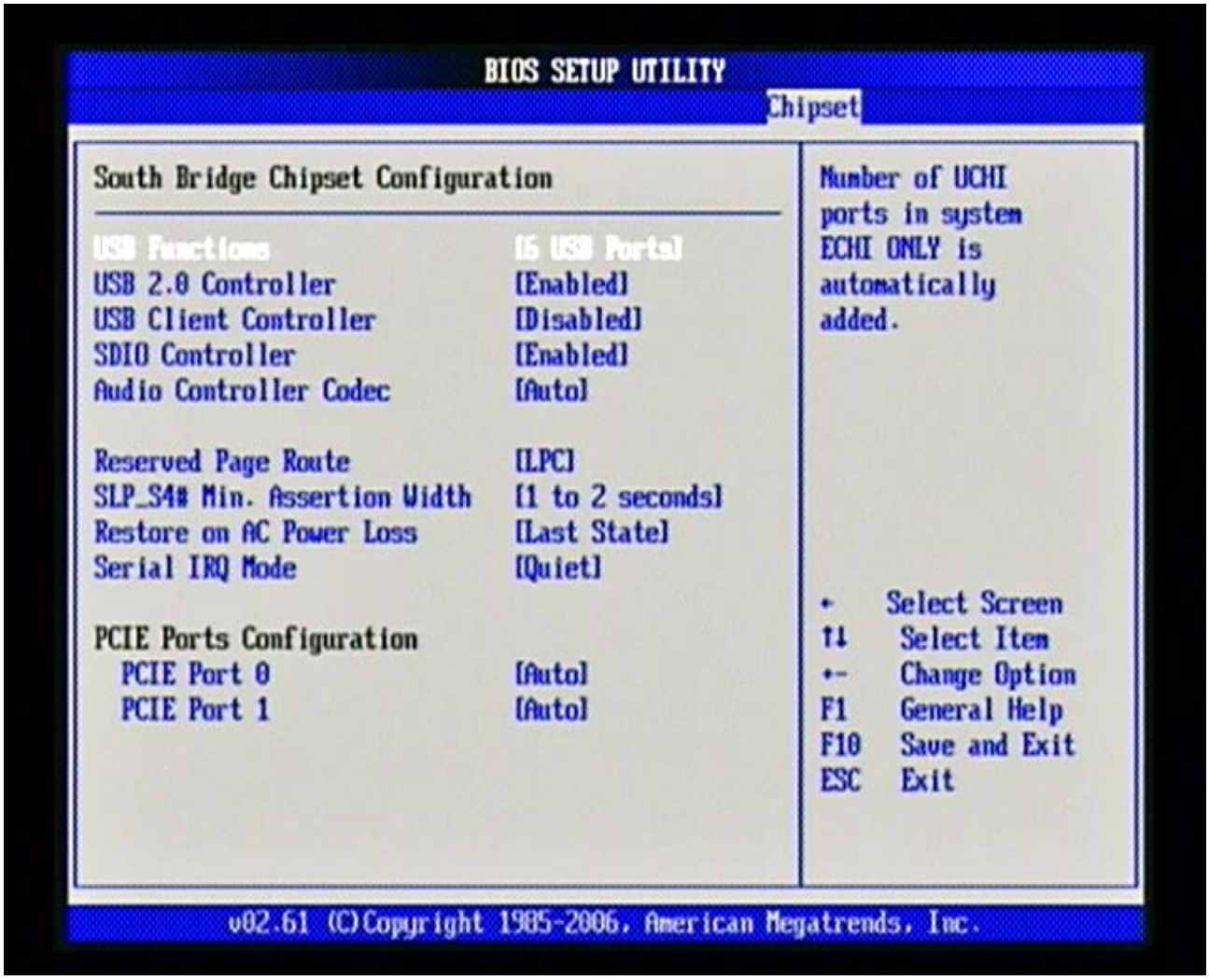
Local Flat Panel Scaling

The choice: Auto, Forced Scaling, Disabled.

Flat Panel Type

The choice: 640x480 18bit (generic), 800x600 18bit (generic), 640x480 24bit (generic), 800x480 24 bit (generic), 1024x768 24bit (generic), 1024x768 18bit (generic), 1280x1024 24bit (generic), 1366x768 (TMD 11.1").

South Bridge Configuration


BIOS SETUP UTILITY
Chipset
South Bridge Chipset Configuration
USB Functions [6 USB Ports]
USB 2.0 Controller [Enabled]
USB Client Controller [Disabled]
SDIO Controller [Enabled]
Audio Controller Codec [Auto]
Reserved Page Route [LPC]
SLP_S4# Min. Assertion Width [1 to 2 seconds]
Restore on AC Power Loss [Last State]
Serial IRQ Mode [Quiet]
PCIE Ports Configuration
PCIE Port 0 [Auto]
PCIE Port 1 [Auto]
Number of UCHI ports in system ECHI ONLY is automatically added.
→ Select Screen
↑↓ Select Item
+- Change Option
F1 General Help
F10 Save and Exit
ESC Exit
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USB Functions

The choice: Disabled, 2 USB Ports, 4 USB Ports, 6 USB Ports.

USB 2.0 Controller

Set to [Enabled] if you need to use any USB 2.0 device in the operating system that does not support or have any USB 2.0 driver installed, such as DOS and SCO Unix.

The choice: Disabled, Enabled.

USB Client Controller

The choice: Enabled, Disabled.

SDIO Controller

The choice: Enabled, Disabled.

Audio Controller Codec

The choice: Auto, Azalia, Disabled.

Reserved Page Route

Determines Port 80h/84-86h/88h/8C-8Eh Route to LPC or PCI.
The choice: PCI, LPC.

SLP_S4# Min. Assertion Width

The choice: 4 to 5 seconds, 3 to 4 seconds, 2 to 3 seconds, 1 to 2 seconds.

Restore on AC Power Loss

This item allows user to configure the power status of using ATX power supply after a serious power loss occurs.

The choice: Power Off, Power On, Last State.

Serial IRQ Mode

The choice: Continuous, Quiet.

PCIE Port 0

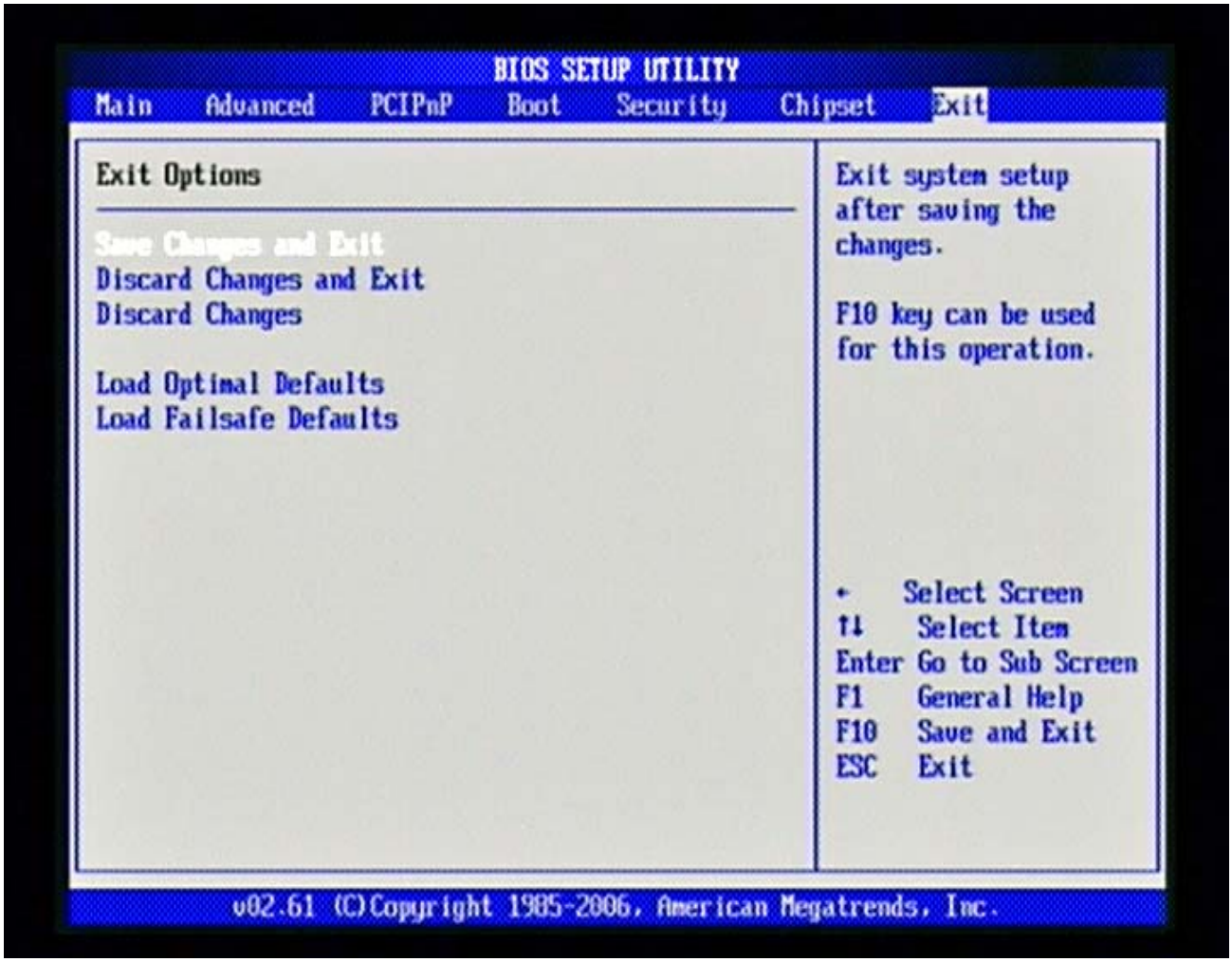
The choice: Auto, Enabled, Disabled.

PCIE Port 1

The choice: Auto, Enabled, Disabled.

4.8 Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.


BIOS SETUP UTILITY
Main Advanced PCIPnP Boot Security Chipset Exit
Exit Options
Save Changes and Exit
Discard Changes and Exit
Discard Changes
Load Optimal Defaults
Load Failsafe Defaults
Exit system setup after saving the changes.
F10 key can be used for this operation.
→ Select Screen
↑↓ Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit
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Save Changes and Exit

Exit system Setup after saving the changes.
Pressing <Enter> on this item asks for confirmation: "Save configuration changes and exit the Setup?"
"F10" key can be used for this operation, too.

Discard Changes and Exit

Exit system setup without saving any changes.
Pressing <Enter> on this item asks for confirmation: "Discard changes and exit setup?"
"Esc" key can be used for this operation, too.

Discard Changes

Discards changes done so far to any of the setup questions.
Pressing <Enter> on this item asks for confirmation: "Discard changes?"
"F7" key can be used for this operation, too.

Load Optimal Defaults

Load Optimal Default values for all the setup questions.
Pressing <Enter> on this item asks for confirmation: "Load Optimal Defaults?"
"F9" key can be used for this operation, too.

Load Failsafe Defaults

Load Failsafe Default values for all the setup questions.
Pressing <Enter> on this item asks for confirmation: "Load Failsafe Defaults?"
"F8" key can be used for this operation, too.

Chapter 5
Troubleshooting

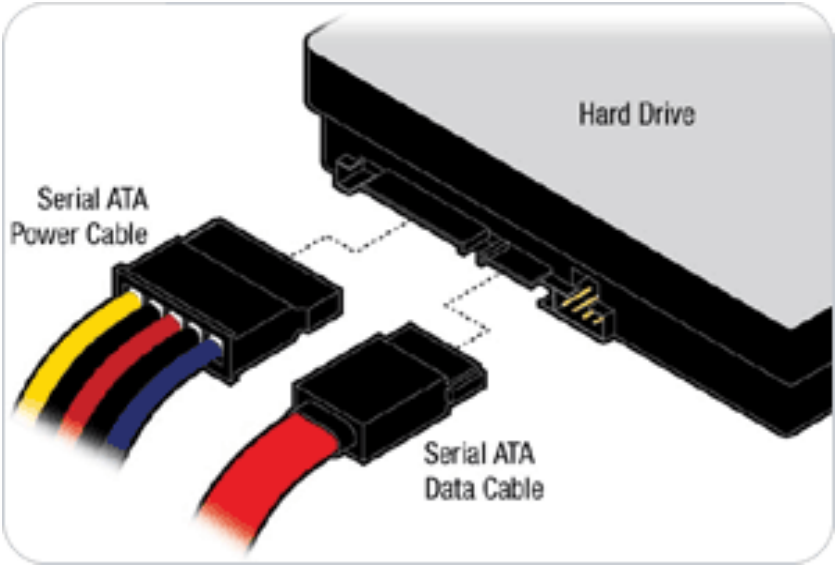
This chapter provides a few useful tips to quickly get PQ7-M103XL running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

DC 12V Power Input

Serial ATA Hard Disk Setting for IDE

Serial ATA channel can only connect to one SATA hard disk at a time; there is single connectors, J3 (PQ7-M103XL). The installation of Serial ATA is simpler and easier than IDE, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation. All you need to do is to plug in two cables and enable SATA in System BIOS.



5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the device cables required before turning on DC 12V power, keyboard, mouse, SATA hard disk, VGA connector, device power cables, 12V DC power accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with PQ7-M103XL, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to "**Load Optimal Defaults**", press "Enter" and "Y" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

Auto Detect Hard Disks

In the BIOS => Advanced=> IDE Configuration menu, pick up any one from Primary Master/Slave IDE ports, and press "Enter". Setup the Type of device to "Auto". This will force system to automatically pick up the IDE devices that are being connected each time system boots up.

Improper disable operation

There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the COM1/ COM2 ports, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are
Disable COM1 serial port to release IRQ #4
Disable COM2 serial port to release IRQ #3
Etc…

A quick review of the basic IRQ mapping is given below for your reference.

IRQ#	Description
IRQ #0	**System Timer**
IRQ #1	**Keyboard Event**
IRQ #2	**Usable IRQ**
IRQ #3	**COM2**
IRQ #4	**COM1**
IRQ #5	**Usable IRQ**
IRQ #6	**Diskette Event**
IRQ #7	**Usable IRQ**
IRQ #8	**Real-Time Clock**
IRQ #9	**Usable IRQ**
IRQ #10	**Usable IRQ**
IRQ #11	**Usable IRQ**
IRQ #12	**IBM Mouse Event**
IRQ #13	**Coprocessor Error**
IRQ #14	**Hard Disk Event**
IRQ #15	**Usable IRQ**

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

5.3 FAQ

Information & Support

Question: What kind of the carrier board which can be inserted by PQ7-M103XL?

Answer: It must use the PQ7-M103XL carrier board to insert the PQ7-M103XL.

If you want to know more, please visit our technical web site at
http://www.portwell.com.tw
For additional technical information, which is not covered in this manual, you can mail to tsd@mail.portwell.com.tw or you can also send mail to our sales, they will be very delighted to forward them to us.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used for your reference.

Memory Area	Size	Description
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0070-0E2E	54K	DOS
0E3F-0F6B	5K	Program Area
0F6C-9FBF	577K	【Available】
First Meg -- Conventional memory end at 639K --		
9FC0-9FFF	1K	Extended BIOS Area
A000-AFFF	64K	Unused
B000-B7FF	32K	VGA Graphics
B800-BFFF	32K	Unused
C000-CE5F	57K	VGA Text
CE60-EFFF	134K	Video ROM
F000-FFFF	64K	Unused
HMA	64K	System ROM

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	**System ROM**	**System Timer**
IRQ 1	**System ROM**	**Keyboard Event**
IRQ 2	**【Unassigned】**	**Usable IRQ**
IRQ 3	**System ROM**	**COM2**
IRQ 4	**System ROM**	**COM1**
IRQ 5	**【Unassigned】**	**Usable IRQ**
IRQ 6	**System ROM**	**Diskette Event**
IRQ 7	**Unused**	**Usable IRQ**
IRQ 8	**System ROM**	**Real-Time Clock**
IRQ 9	**【Unassigned】**	**Usable IRQ**
IRQ 10	**【Unassigned】**	**Usable IRQ**
IRQ 11	**【Unassigned】**	**Usable IRQ**
IRQ 12	**System ROM**	**IBM Mouse Event**
IRQ 13	**System ROM**	**Coprocessor Error**
IRQ 14	**System ROM**	**Hard Disk Event**
IRQ 15	**【Unassigned】**	**Usable IRQ**